A Power-Efficient Wireless Neural Stimulating System with Inductive Power Transmission

A Dissertation

Presented to

The Academic Faculty

By

Hyung-Min Lee

In Partial Fulfillment

Of the Requirements for the Degree

Doctor of Philosophy in the

School of Electrical and Computer Engineering

Georgia Institute of Technology

May 2014

A Power-Efficient Wireless Neural Stimulating System with Inductive Power Transmission

Approved by:

Dr. Maysam Ghovanloo, Advisor
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Pamela Bhatti
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Farrokh Ayazi
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Wen Li
School of Electrical and Computer Engineering
Michigan State University

Dr. Hua Wang
School of Electrical and Computer Engineering
Georgia Institute of Technology

Date Approved: Mar. 26, 2014

To my family

ACKNOWLEDGEMENTS

I would like to express my sincere gratitude and appreciation to my advisor, Dr. Maysam Ghovanloo for his generous guidance and overwhelming support. I really have learned a lot from him about not only research but also enthusiasm, dedication, and professionalism in his work. It was my greatest luck and pleasure to join the GT-Bionics lab and work with him during my Ph.D. period. His advisorship gave me a significant and positive impact for my future career and even life.

I would like to thank Dr. Farrokh Ayazi and Dr. Hua Wang for their time and consideration in reviewing my Ph.D. thesis and serving as reading committee members. Their valuable comments and feedback have been really helpful to further improve my research. In addition, I am grateful to the rest of my committee members, Dr. Pamela Bhatti and Dr. Wen Li for being generous in sharing their expertise and valuable advice.

During 5 years in Georgia Tech, a lot of people helped me not only do research and pursue Ph.D. degree but also even live in Atlanta. Especially, I would like to thank GT-Bionics lab members for their full contributions. They have truly inspired me in all the good and bad times and supported me in every stage of my research. Indeed, they were sincere friends and great collaborators who have fully motivated me.

Last, but the most important, I would thank my family: my parents, my brother, my wife, and my little daughter. Their endless love and support make me complete this long trip. I really thank my wife, Hyunyoung, for being with me. I am grateful to her for pulling me through difficult times with her unconditional love. I would never complete my Ph.D. thesis without her support and encouragement. I love you.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

SUMMARY

The objective of the proposed research is to advance the power efficiency of wireless neural stimulating systems in inductively powered implantable medical devices (IMD). Several innovative system- and circuit-level techniques are proposed towards the development of power-management circuits and wireless neural stimulating systems with inductive power transmission to improve the overall stimulation power efficiency.

Neural stimulating IMDs have been proven as effective therapies to alleviate neurological diseases, while requiring high power efficiency and performance for more efficacious treatments. Inductive power transmission across the skin is currently the only viable solution for providing sufficient power to such IMDs without imposing size and power constraints of implanted batteries. Therefore, power-management circuits in IMDs should have high power conversion efficiency (PCE) to operate with smaller received power from a larger distance. Neural stimulating systems are also required to have high stimulation efficiency for activating the target tissue with a minimum amount of energy from the inductive link while ensuring charge-balanced stimulation, providing several advantages such as a wide range of stimulus energy, a long battery life in an external power transmitter (Tx), extended-range inductive power transmission, efficacious and safe stimulation, and less tissue damage from overheating.

The proposed research presents three approaches to design and implement the power-efficient wireless stimulating IMDs: 1) optimized power-management circuits for inductively powered biomedical microsystems, 2) a power-efficient neural stimulating system with adaptive supply control, and 3) a wireless switched-capacitor stimulation (SCS) system, which is a combination of power-management circuits and the neural stimulating system, to maximize both stimulator efficiency (before electrodes) and stimulus efficacy (after electrodes).

The contributions from this research work are summarized as follows:

1. Development of power-efficient active AC-to-DC converters for inductively powered applications
2. Development of an adaptive reconfigurable voltage doubler/rectifier (VD/REC) for extended-range inductive power transmission
3. Development of power-management circuits in wireless biomedical microsystems
4. Development of a compact distributed stimulating system for multichannel deep brain stimulation (DBS)
5. Development of an adaptive wireless neural stimulating system with closed-loop supply control
6. Development of a wireless capacitor charging system through inductive links
7. Development of a power-efficient wireless switched-capacitor stimulating (SCS) system for electrical and optical stimulation
8. Proposing a tissue model for electrical stimulation and analysis for energy-efficient stimulus waveform shape
9. *In vivo* animal experiments with the SCS system for electrical stimulation and wireless optogenetics

CHAPTER I

INTRODUCTION

1.1. Motivation

Implantable microelectronic devices (IMD) have already been used successfully in the form of cochlear implants to substitute a sensory modality (hearing) that might be lost due to diseases or injuries [1]. More recent IMD applications demand higher performance and power efficiency to enable very sophisticated treatment paradigms, such as retinal implants for the blind or bidirectional cortical brain-computer-interfaces (BCI) with sensory feedback for amputees or those suffering from severe paralysis [2]-[5]. These IMDs require more power to handle more functions on a larger scale, particularly when they need stimulation through a large number of electrodes at high rates, which power level is less dependent on the circuit efficiency [6], [7]. Therefore, the new IMD power consumption is going to be orders of magnitude higher than traditional IMDs, *e.g.* pacemakers [8].

In most cases, supplying the IMDs with primary batteries will not be an option because of their large volume, limited lifetime, replacement hardship, and cost [9]. Inductive power transmission across the skin is currently the only viable solution to overcome size, cost, and longevity while providing sufficient power to such IMDs [6], [10]-[12]. Considering that the temperature at the outer surface of the IMD should not increase more than 2 °C for the surrounding tissue to survive [13], it is of utmost importance for the inductive link and the IMD power management circuitry to maintain very high power transfer efficiency. There are also other applications such as inductively powered mobile device chargers, radio-frequency identification (RFID), and near-field communication (NFC), in which high power efficiency and robustness through weak inductive links are highly desired [14]-[16]. Fig. 1.1 shows some of the aforementioned applications for inductive power transmission.

(a) (b) (c) (d)

Fig. 1.1. Different applications for inductive power transmission. (a) A cochlear implant [1], (b) A visual prosthesis [4], (c) A mobile device charger [14], and (d) An NFC device [16].

The inductively powered IMD can be also utilized for neuroscience research applications that are used on freely moving animal subjects, as shown in Fig. 1.2. Conventional battery-powered IMDs need to replace internal batteries periodically while size and weight of the batteries tether animal's movements and affect their behavior, limiting the long-term awake animal experiments. However, wireless power transmission through the inductive link enables the inductively powered IMD to operate for long-term uninterrupted electrophysiology experiments on small freely moving animals.

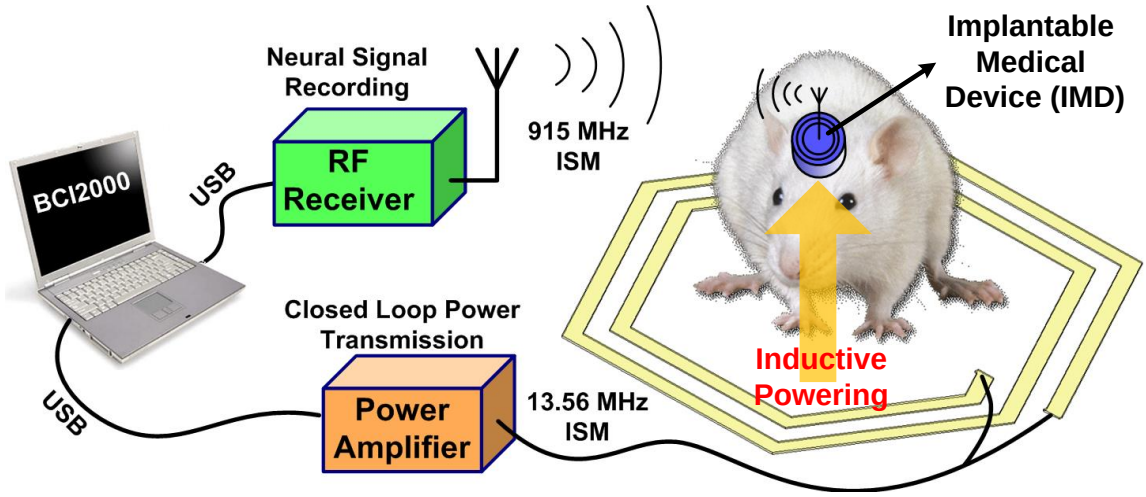


Fig. 1.2. Long-term freely moving animal experiment setup with the inductively powered IMD.

In addition to the inductive power transmission capability, the IMDs need to adopt aggressive power management schemes to further improve the power efficiency, especially for high-power stimulating IMDs. While stimulating IMDs need to provide a

wide range of stimulus energy to the tissue, the power transferred through the inductive link is typically limited due to the size constraint of the implantable secondary coil [17]. Therefore, to improve the overall efficiency of the inductively powered stimulating IMD, the efficiencies of every stage of the power delivery path, such as the inductive link, power-management circuit, stimulating system, and even stimulus waveform to the tissue, should be maximized by utilizing energy-efficient system- and circuit-level techniques.

1.2. Background

The power conversion efficiency (PCE) of the AC-to-DC converter is a key factor in improving the overall power efficiency of the system because the received power from the inductive link needs to pass through it before being delivered to the IMD. Since the rectified output voltage, V_{OUT}, may vary significantly with the changes in coils' relative distance and alignment, a low-dropout regulator (LDO) often follows the AC-to-DC converter to provide a constant supply voltage, V_{DD}, to the IMD load.

Fig. 1.3 shows the inductive power transmission flow from the external power source to the IMD through the inductive link [17]. Considering the power flow from the external transmitter (Tx) to the IMD load and the potential regulator, the total PCE, η_{Total}, can be calculated from,

$$\eta_{Total} = \eta_{PA} \times \eta_{Link} \times \eta_{ACDCC} \times \eta_{Regulator} \tag{1.1}$$

where η_{PA}, η_{Link}, η_{ACDCC}, and $\eta_{Regulator}$ are the efficiencies of the power amplifier, inductive link, AC-to-DC converter, and regulator, respectively [17]. In Fig. 1.3, $\eta_{PA} = \eta_S$, $\eta_{Link} = \eta_1 \times \eta_T \times \eta_2$, and $\eta_{ACDCC} \times \eta_{Regulator} = \eta_L$. Achieving higher PCE ($\eta_{Total}$) is very important in inductively powered applications because it allows IMDs to operate with smaller received power from a larger distance. Lower received power also reduces the risk of tissue damage from overheating [13]. In the IMD applications, η_{Link} is limited due to the size constraint of the secondary coil [17]. The regulator, on the other hand, already has a

high efficiency, $\eta_{Regulator}$, because of its low dropout. Therefore, improving the AC-to-DC converter PCE (η_{ACDCC}) is key for safe and power-efficient IMD operation.

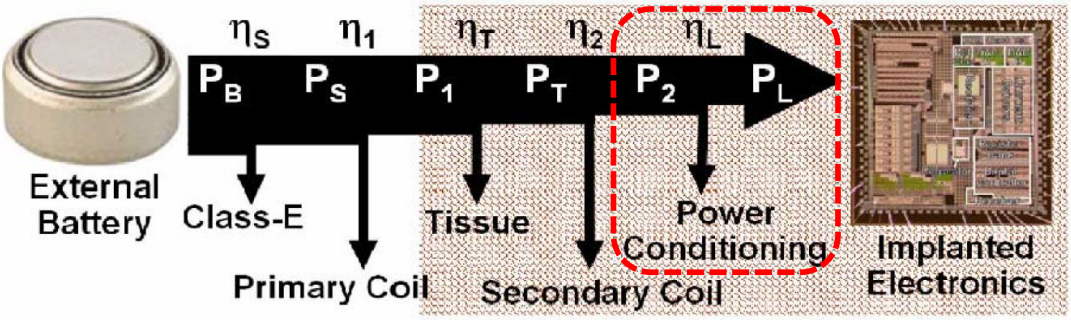


Fig. 1.3. Inductive power transmission flow from external power source to the IMD [17].

Among a variety of AC-to-DC converters, passive rectifiers and voltage doublers using diode-connected transistors suffer from large forward voltage drops and power losses because of their threshold voltages, resulting in low PCE [9], [12], [18]-[21]. A bridge rectifier using Schottky diodes has low dropout voltage [22], but it has high leakage current and it is not available in a standard CMOS process without extra fabrication steps. In addition, its reverse breakdown voltage may not be high enough for stimulation applications. Several threshold-voltage (V_{Th}) compensation techniques have been proposed to reduce the forward voltage drop by adjusting effective V_{Th} in passive rectifiers, voltage doublers, and multipliers [23]-[28]. However, they still need to deal with several issues such as sensitivity to process variations, leakage, and back currents.

Active synchronous rectifiers using comparator controlled rectifying switches are currently considered the most promising solutions for increasing the PCE of AC-to-DC converters [29]-[42]. In these rectifiers, voltage drop across the main rectifying switches is much lower than the diode voltage drop, dissipating less power within the rectifier and achieving high PCE. However, those rectifiers suffer from turn-on and turn-off delays of comparators at higher carrier frequencies, such as 13.56 MHz in the industrial, scientific, and medical (ISM) band, resulting in forward conduction delay as well as back-current

power loss. In addition, their peak input voltages, which may be significantly limited by weakly-coupled inductive links, need to be always higher than the desired output voltages, resulting in lower operating range or higher voltages on the Tx side. To address such limitations, comparator-based active voltage doublers have been proposed [43], [44]. However, these topologies only operate at low frequencies (<1 kHz) in applications such as energy scavenging from vibrations using piezoelectric transducers.

Therefore, improved active AC-to-DC converters are required for IMDs with inductive links that operate within the high-frequency (HF) band, while achieving higher PCE with extended power-transmission range. Moreover, the power-management circuits in inductively powered IMDs need to accommodate a wider range of coil misalignments and distance variations for robust and reliable inductive power transmission.

Recently, IMDs with stimulating function have been proven as effective therapies to alleviate neurological diseases or substitute sensory modalities lost due to diseases or injuries [45]-[47]. These implantable stimulators are capable of injecting a designated amount of charge into the human body (often the neuronal tissue) by providing a precise amount of output current or output voltage for a predefined period. Deep brain stimulation (DBS) is one of the most effective examples of such therapies to treat Parkinson's disease, tremor, and dystonia [48], [49]. Today's DBS devices use large primary batteries implanted in the chest area, where there is more space available, and their subcutaneous interconnects pass across the neck to reach the electrodes implanted deep in the brain, as shown in Fig. 1.4 [50]. Batteries need to be replaced every 2 ~ 5 years through surgery, and there is always risk of mechanical failure in interconnects due to head motion. A head-mounted DBS can eliminate hardship imposed by chest-implanted primary batteries and long interconnects across the neck, replacing them with transcutaneous inductive power transmission from a behind the ear (BTE) rechargeable energy source, similar to cochlear implants and hearing aids [1], [10]-[12].

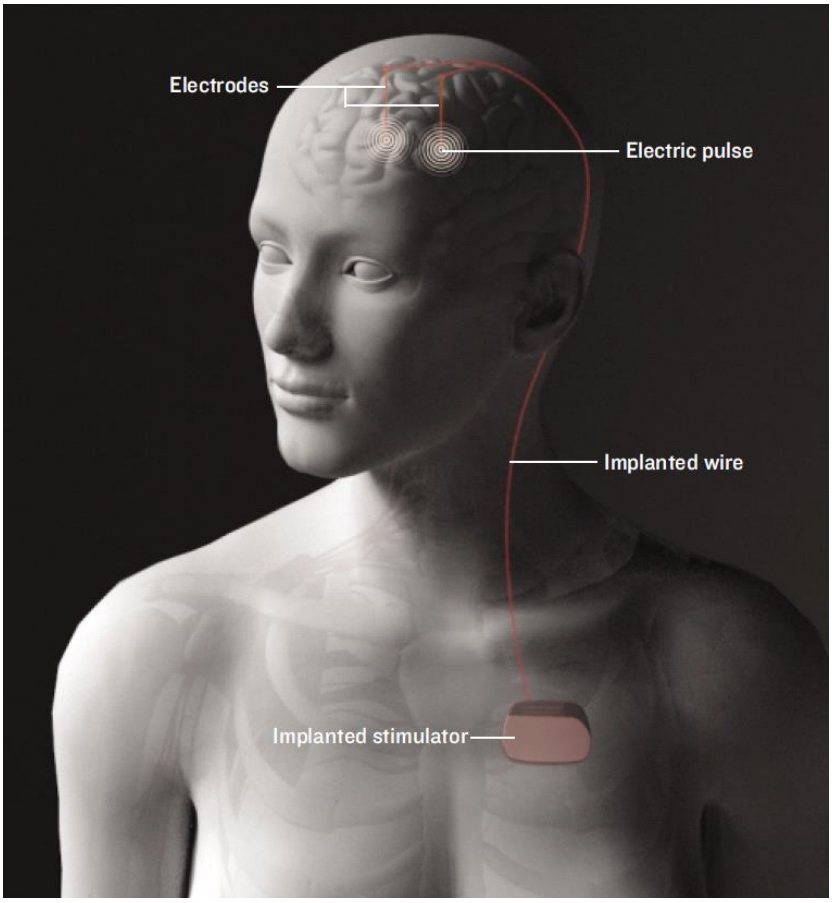


Fig. 1.4. Chest-implanted battery-powered deep brain stimulator [50].

Fig. 1.5 shows the conceptual configuration of a head-mounted inductively powered DBS system as opposed to the conventional chest-implanted battery-powered DBS in Fig. 1.4. The external processing unit, which includes a rechargeable battery, provides transcutaneous power and data through a pair of loosely-coupled coils. The induced AC input across the implanted coil supplies the rest of the DBS implant through an efficient power-management unit. The DBS system generates stimulus pulses, which are delivered to the stimulation sites via individual leads that are significantly shorter than those from the chest area, and therefore, less invasive and more suitable for high-density DBS [51]. Like other wirelessly-powered IMDs, high power efficiency is paramount in reducing the risk of tissue damage from overheating [13].

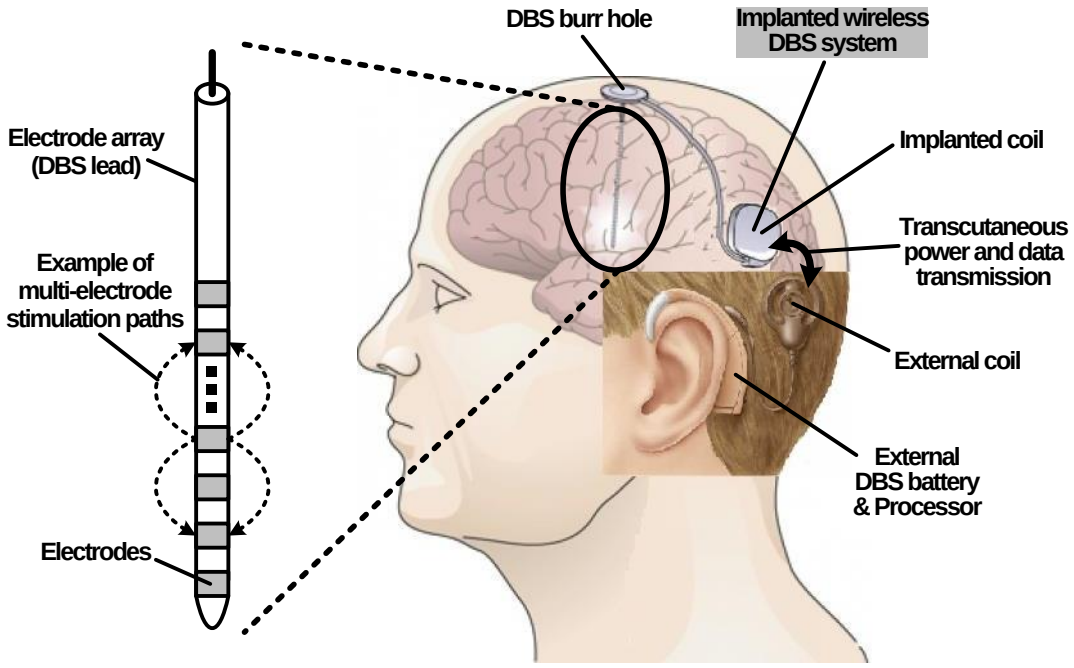


Fig. 1.5. Conceptual configuration of a head-mounted inductively powered DBS system in which power and data are transferred through the inductive link.

Typically, three types of stimulation mechanism have been utilized depending on the application: voltage-controlled stimulation (VCS), current-controlled stimulation (CCS), and switched-capacitor stimulation (SCS) [52]. While VCS enables power-efficient stimulation, tissue and electrodes impedance needs to be known accurately to control the stimulation charge [52]. Balancing the stimulation charge is quite complicated in VCS because the electrode impedance varies over time and position. If the residual charge, which accumulates in the tissue following stimulation pulses, exceeds a safe limit, electrolysis of extracellular fluid can lead to pH variations, causing both tissue and electrode damage [49]. Conversely, CCS has been widely used because of its precise charge control and safe operation [53]. However, traditional CCS has low power efficiency due to the dropout voltage across the current source, which can result in significant power loss depending on the stimulation site voltage. SCS takes advantages of both high efficiency and safety by using capacitor banks to store and transfer charge to the tissue [52], [54]. However, it requires several off-chip capacitors that may increase

the IMD size. In addition, a high-efficiency capacitor-charging circuit with an AC input is needed to improve the overall DBS efficiency.

Fig. 1.6 compares various inductively powered stimulating structures, while all structures were assumed to provide bipolar and biphasic stimulation through a similar pair of electrodes. We have assumed that the inductive link can maintain its peak efficiency against reflected impedance variations as stimulator loading changes by utilizing a multi-coil inductive link or an adaptive resonant load transformation [55], [56]. Here we focus on power efficiency of the stimulating IMD, which can be defined as the ratio of the AC input power from the secondary coil to the stimulator output power delivered to the tissue.

The conventional inductively powered CCS in Fig. 1.6a utilizes a rectifier to convert the AC input to a DC V_{REC}, followed by a low-dropout regulator (LDO) to generate a fixed supply voltage, V_{DD} [47]. This simple structure wastes a large portion of the input power across the LDO, which is needed to accommodate V_{REC} variations, and the current source, while the loss increases as V_{STIM}, the required voltage to maintain stimulation current constant, becomes smaller. Lee proposed the fixed output rectifier in Fig. 1.6b to generate a predefined constant V_{REC} without an LDO [57]. Eliminating the LDO reduced the loss, but the CCS loss was still dominant during stimulation, especially when $V_{STIM} << V_{REC}$.

The stimulator in [58] utilized a dynamic supply, V_{IN}, from a DC-DC converter as shown in Fig. 1.6c. It achieved high efficiency from VCS as well as coarse current controllability. However, it still required constant DC input, V_{REC}, from the rectifier, which loss should be added to that of the DC-DC converter (η_{DCDC} = 55 ~ 94%). In Fig. 1.6d, the inductive power delivered to the stimulator was adjusted through an external closed loop, changing V_{REC} to be near the peak voltage of V_{STIM}, leading to small power loss in CCS current sources [59], [60]. However, the external control loop via load-shift-keying (LSK), which adjusts the inductive power transmission, is prone to interference

and can even be interrupted in a loosely-coupled inductive link, while increasing the system complexity. The passive rectifier also induced large AC-DC loss, which decreased the overall power efficiency [12]. While individually they suffer from their limitations, the methods used in these inductively powered stimulating structures may be used together to further improve the power efficiency.

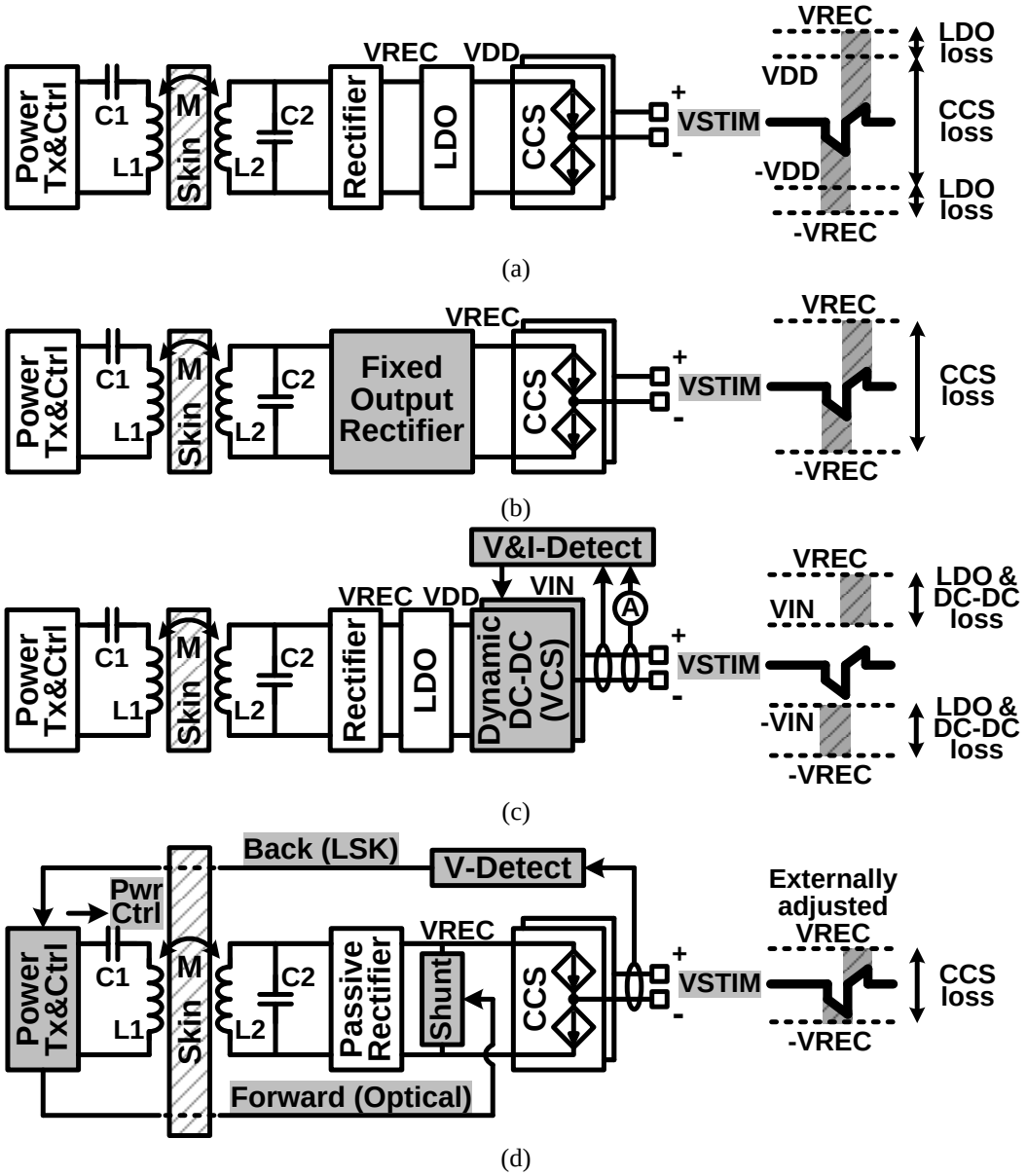


Fig. 1.6. Various inductively powered stimulating structures with (a) the conventional rectifier and regulator [47], (b) the fixed output rectifier [57], (c) the dynamic dc-dc converter [58], and (d) the external closed loop supply control [59], [60].

Therefore, the inductively powered stimulating IMD needs to improve its stimulation power efficiency by adopting innovative system- and circuit- level techniques, while receiving the limited power through the inductive link. Moreover, the shape of the stimulus waveform, which is provided to the tissue, can be also adjusted to further improve the stimulus efficiency (after electrodes) in addition to the stimulator efficiency (before electrodes) [61], [62].

1.3. Dissertation Outline

This dissertation has been organized as follows: Chapter 2 presents power-efficient AC-to-DC converters, which are an active rectifier and active voltage doubler, by utilizing offset-controlled comparators for inductively powered applications. Chapter 3 proposes an adaptive reconfigurable voltage doubler/rectifier (VD/REC) for extended-range inductive power transmission. Chapter 4 details the power-management circuits for wireless power and data transmission in various biomedical microsystems. Chapter 5 describes a compact wireless neural stimulating system with distributed stimulators for multichannel deep brain stimulation (DBS). Chapter 6 provides an adaptive wireless neural stimulating system with closed-loop supply control for power-efficient DBS. Chapter 7 proposes a novel power-efficient switched-capacitor stimulating (SCS) system for electrical and optical DBS. Chapter 8 presents tissue modeling and efficiency analysis for various stimulus waveform shapes, while demonstrating *in vivo* animal experiments with the SCS system for both electrical stimulation and wireless optogenetics. Chapter 9 discusses the conclusion and future works.

CHAPTER II

POWER-EFFICIENT AC-TO-DC CONVERTERS FOR INDUCTIVELY POWERED APPLICATIONS

2.1. Introduction

In inductively powered implantable medical devices (IMD), the power conversion efficiency (PCE) of the AC-to-DC converter is key in improving the overall system power efficiency and heat dissipation because all the received power from the inductive link needs to pass through it before being delivered to the IMD. With higher PCE, the IMDs can operate with smaller received power from a larger coils' separation, while reducing the risk of tissue damage from overheating.

This chapter presents fully-integrated power-efficient active AC-to-DC converter solutions that can be used between the inductive link and the IMD at high carrier frequency: active rectifier and active voltage doubler. Each of these AC-to-DC converters suits a certain application depending on specs, such as peak input voltage, PCE, dropout voltage, operating frequency, delivered power capacity, IMD supply voltage, and power transmission range. All AC-to-DC converters utilize active diodes which rectifying switches are driven by offset-controlled high-speed comparators to reduce the voltage drop and power loss. Offset-control function in comparators can compensate for both turn-on and turn-off delays to drive the rectifying switches at optimal times particularly in high frequency bands. Hence, the proposed active rectifier and voltage doubler can achieve high PCEs at high frequency range of 13.56 MHz. These AC-to-DC converters, which are all CMOS compatible, can be utilized in various inductively powered IMDs to provide sufficient power through weakly coupled inductive links.

A generic inductively powered IMD consists of three main components: a power transmitter (Tx), an inductive link, and an IMD, as shown in Fig. 2.1. On the Tx side, a power amplifier (PA) drives the primary coil, L_1, at the carrier frequency, f_c. This signal is induced on to the secondary coil, L_2, through the inductive link, and generates an AC

input voltage, V_{IN}, across the resonance circuit, L_2 and C_2. The L_2C_2 tank is always followed by an AC-to-DC converter to provide the rest of the IMD with a DC output voltage, V_{OUT}. A variety of AC-to-DC structures can be used between the inductive link and the IMD: passive rectifiers, passive voltage doublers or multipliers, active rectifiers, and active voltage doublers, as shown in Fig. 2.1. Each AC-to-DC converter structure suits a certain application depending on specifications such as peak input voltage, power conversion efficiency (PCE), dropout voltage, operating frequency, delivered power capacity, and size of the IMD.

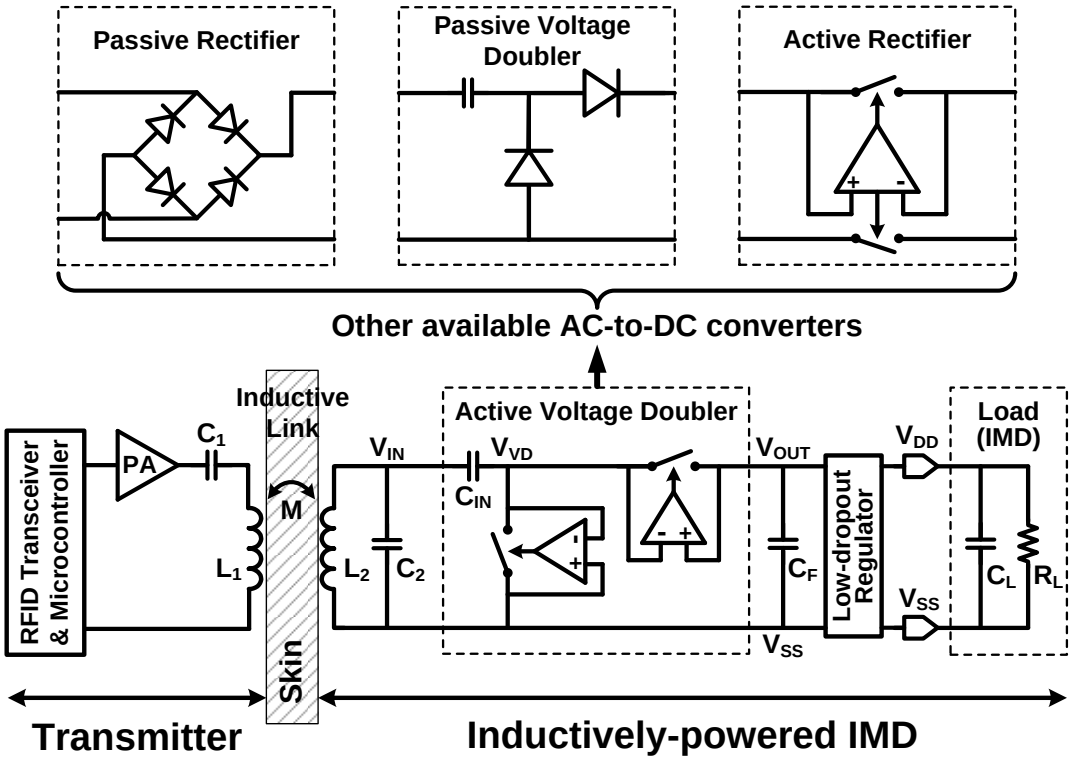


Fig. 2.1. Block diagram of an inductively powered implantable medical device (IMD) with emphasis on the power transmission through the AC-to-DC converter.

2.2. Active Rectifier

2.2.1. Active Rectifier Architecture

The new full-wave active rectifier employs a pair of high-speed comparators (CMP_1 and CMP_2) to drive the main rectifying elements (P_1 and P_2) in Fig. 2.2. Ideally,

the input voltage of the rectifier, $V_{IN} = V_{IN1} - V_{IN2}$, has a sinusoidal waveform. Hence, P_1 and P_2 turn on alternatively depending on the polarity and amplitude of V_{IN}.

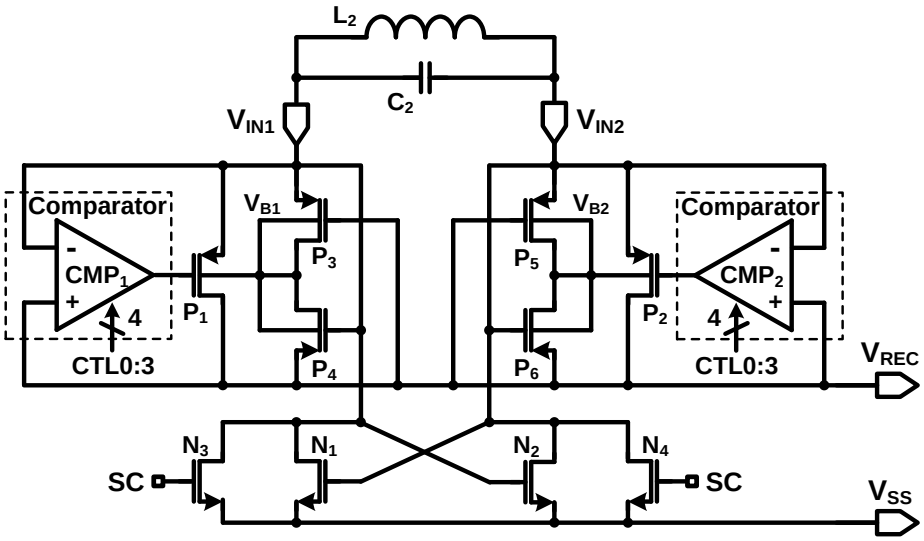


Fig. 2.2. Schematic diagram of our active rectifier including offset-controlled high speed comparators, dynamic body biasing, and load shift keying (LSK) back telemetry functions.

When $V_{IN} > V_{ThN}$ (the NMOS threshold voltage) and $|V_{IN}| < V_{REC}$, the positive feedback operation of the cross-coupled NMOS pair (N_1 and N_2) connects V_{IN2} to V_{SS} through N_2 and turns off N_1. In this case, CMP_2 output goes high because $V_{REC} > V_{SS}$, and P_2 is turned off. P_1 also remains off as long as $|V_{IN}| < V_{REC}$. When $|V_{IN}| > V_{REC}$, CMP_1 output goes low and turns P_1 on. Therefore, current flows from V_{IN1} to V_{REC}, and charges the rectifier's resistive/capacitive load (R_LC_L). In the next half cycle, when $V_{IN} < -V_{ThN}$, V_{IN1} is connected to V_{SS} through N_1, N_2 turns off, and both P_1 and P_2 are also initially off for the period of $|V_{IN}| < V_{REC}$. Then, after $|V_{IN}| > V_{REC}$, CMP_2 turns P_2 on and current flows from V_{IN2} to V_{REC} to charge the resistive/ capacitive load again.

To avoid latch-up and substrate leakage problems among P_1 and P_2, potentials at their separated N-well body terminals (V_{B1} and V_{B2}) need to be the highest potentials on-chip. We adopted the dynamic body bias control technique from [18] and [63] by utilizing auxiliary PMOS transistors, P_3 to P_6. With this method, V_{B1} and V_{B2} are automatically connected to the highest potential between the input voltages, V_{IN1} and V_{IN2},

and the output voltage, V_{REC}, of the rectifier.

2.2.2. Power Conversion Efficiency (PCE) Analysis

The PCE of the active rectifier depends on the size of the rectifying PMOS and the cross-coupled NMOS pairs because these transistors are in the main current path. For example, when V_{IN1} - V_{IN2} > V_{REC}, P_1 and N_2 turn on and open a current path to the load, as shown in Fig. 2.3.

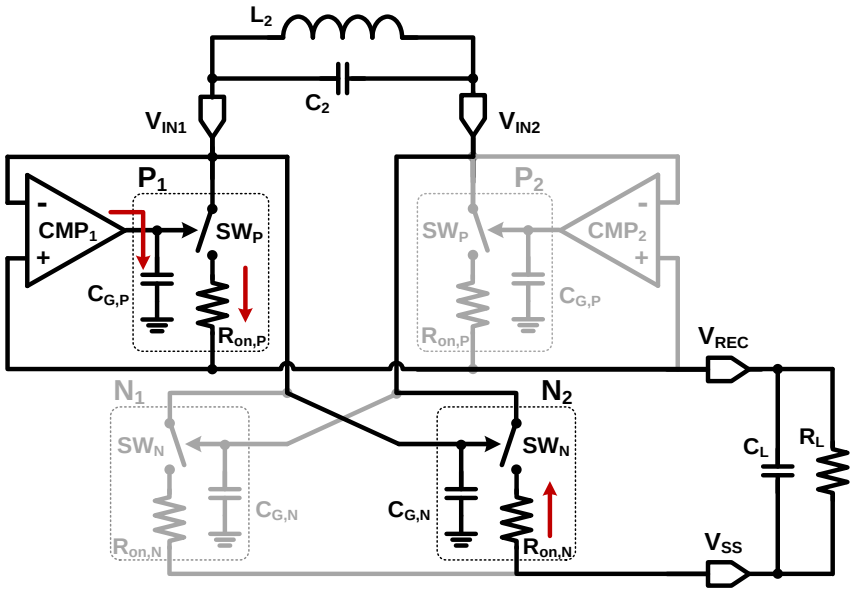


Fig. 2.3. Simplified schematic diagram of the active rectifier depicting the current path and power dissipating components when V_{IN1} - V_{IN2} > V_{REC}.

In this case, the total lost power, $P_{Loss,total}$, will be dominated by the switching loss of P_1 ($P_{Loss,Cgp}$), R_{on} loss of P_1 ($P_{Loss,Ronp}$), and R_{on} loss of N_2 ($P_{Loss,Ronn}$). Since the gate of N_2 is always connected to the input node of the rectifier, there is negligible switching loss for charging and discharging the gate capacitance of N_2. Therefore, $P_{Loss,total}$ can be approximated by,

$$P_{Loss,total} = P_{Loss,C_{gp}} + P_{Loss,R_{onp}} + P_{Loss,R_{onn}} = C_{gp}V_{REC}{}^2 2f_c + I_p{}^2 R_{onp}D_{eff} + I_n{}^2 R_{onn}D_{eff}$$
$$= W_p C^*_{gp} V_{REC}{}^2 2f_c + \left(\frac{V_{REC}}{R_L D_{eff}}\right)^2 D_{eff}\left(R_{onp} + R_{onn}\right) \quad (2.1)$$

where C^*_{gp} is the gate capacitance per unit width of P_1, f_c is the carrier frequency (= 13.56

MHz), D_{eff} is the effective duty cycle including comparator delays, and W_p is the width of P_1.

In this design, we have assumed $W_n = W_p$ for the sake of simplicity. However, we have also proven in [64] that the optimal size ratio of the PMOS and NMOS transistors can be found from,

$$\left(\frac{W_p}{W_n}\right)_{opt} = \sqrt{\frac{K_n \cdot (V_{REC} - V_{ThN})}{K_p \cdot (V_{REC} - |V_{ThP}|)}} \tag{2.2}$$

where $K_p = \mu_p C_{ox}$ and $K_n = \mu_n C_{ox}$ are the PMOS and NMOS transconductances, respectively. One should note that even though larger transistor size decreases the R_{on} loss, it increases the switching loss and comparator delays due to the larger gate capacitance. Therefore, the main rectifying transistors have an optimal size for minimum power dissipation depending on f_c and R_L, which should also comply with the total chip area that is allocated to the rectifier [64].

T_{PHL} and T_{PLH}, the turn-on and turn-off delays of $CMP_{1,2}$, affect the rectifier PCE because these delays hinder $P_{1,2}$ switches from turning on and off at proper times and cause back current. Our model considers the size of the rectifying transistors and comparator delays to estimate the maximum PCE. In the Appendix, we have defined W_p, $R_{onp} + R_{onn}$, and D_{eff} as functions of the switching duty cycle (D), T_{PHL}, and T_{PLH}, and differentiated (2) with respect to D to minimize $P_{Loss,total}$. With the power loss from (2), we can estimate the maximum PCE of the rectifier,

$$\eta_{rectifier} = \frac{P_{Load}}{P_{Load} + P_{Loss,total} + 2P_{Comparator}} \tag{2.3}$$

where P_{Load} is the output power, and $P_{Comparator}$ is the total power consumption of each comparator excluding the charging and discharging power consumption of $P_{1,2}$ gates, which has already been considered in $P_{Loss,total}$.

Fig. 2.4 shows the calculated rectifier PCE vs. W_p for various comparator delays, using parameters from the ON Semi 0.5-μm standard CMOS process.

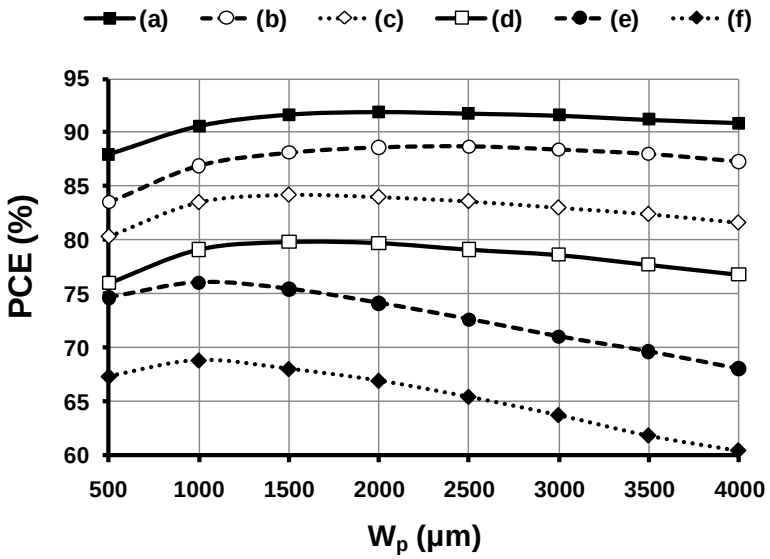


Fig. 2.4. Calculated rectifier power conversion efficiency (PCE) vs. W_p depending on the comparator delays when V_{REC} = 3.2 V and R_L = 500 Ω. Curve-a: T_{PHL} = 0 ns and T_{PLH} = 0 ns, Curve-b: T_{PHL} = 5 ns and T_{PLH} = 0 ns, Curve-c: T_{PHL} = 0 ns and T_{PLH} = 3 ns, Curve-d: T_{PHL} = 3 ns and T_{PLH} = 3 ns, Curve-e: T_{PHL} = 0 ns and T_{PLH} = 4 ns, and Curve-f: T_{PHL} = 4 ns and T_{PLH} = 4 ns.

In this calculation, we assume that P_{Load} = 20 mW, V_{REC} = 3.2 V, R_L = 500 Ω, and $P_{Comparator}$ = 0.1 mW, which are based on the simulation results. It can be seen that with W_p = 2100 μm and T_{PHL} = T_{PLH} = 0 ns, the rectifier achieves the highest PCE of 92%. This is the theoretical upper limit for the PCE that can be obtained by choosing optimized transistor width and eliminating the effect of comparators' delay by utilizing offset-controlled high speed comparators that are described in the next section.

2.2.3. Offset-controlled High-speed Comparators

In order to drive the large rectifying PMOS transistors at high operating frequency of 13.56 MHz, high speed comparators with low power consumption and high driving capability are required. Typically, the comparator operating speed is limited by its propagation delay, T_P, which is how quickly the output responds to a change at the input. In this rectifier application, the comparator propagation delay adversely affects the PCE. Due to T_{PHL}, the comparators turn $P_{1,2}$ on too late and reduce the input power that could otherwise be transferred to the load during this delay. Moreover, due to T_{PLH}, comparators lag in turning $P_{1,2}$ off, and current can instantaneously flow from C_L back to

the secondary coil when $V_{IN} < V_{REC}$.

Since it is not possible to reduce T_P to zero, in order to overcome such limitations, we have utilized offset control function in the high speed comparators used in this rectifier. Fig. 2.5 shows the block diagram of this comparator, which consists of a common-gate type comparator (CG Cmp), two offset-control blocks ($Offset_F$ and $Offset_R$), and current-starved (CS) inverters. Offset-control blocks inject a programmable offset current, OS_F and OS_R, to the inputs of the CG comparator alternately depending on the state of the V_{OUT} feedback signals, FB_F and FB_R. Therefore, V_{OUT} expedites the falling or rising transition by sensing them ahead of time.

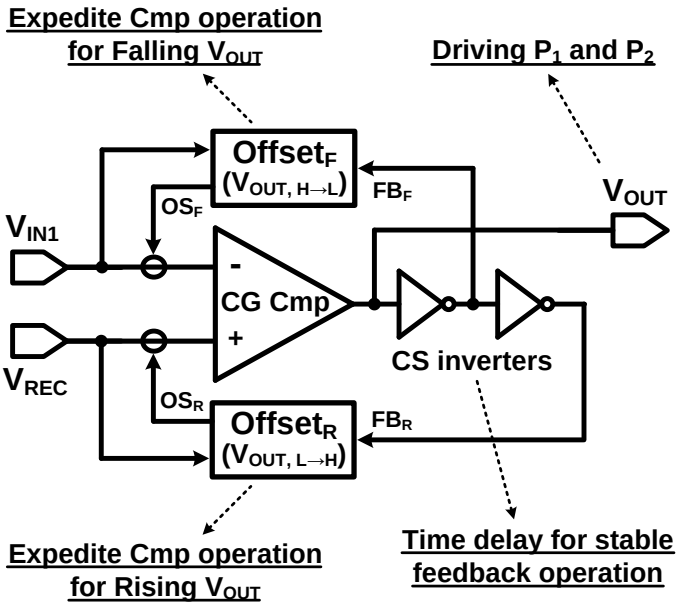


Fig. 2.5. Block diagram of the high speed comparator employing offset control functions for both falling and rising V_{OUT} transitions.

Fig. 2.6 shows the schematic diagram of the high speed comparator with two offset-control functions, $Offset_F$ and $Offset_R$. Without considering offset-control blocks and CS inverters, it basically works as a simple common-gate comparator with start-up capability [29]. Two input voltages, V_{REC} and V_{IN1}, are applied to the sources of input transistors, P_7 and P_8, respectively.

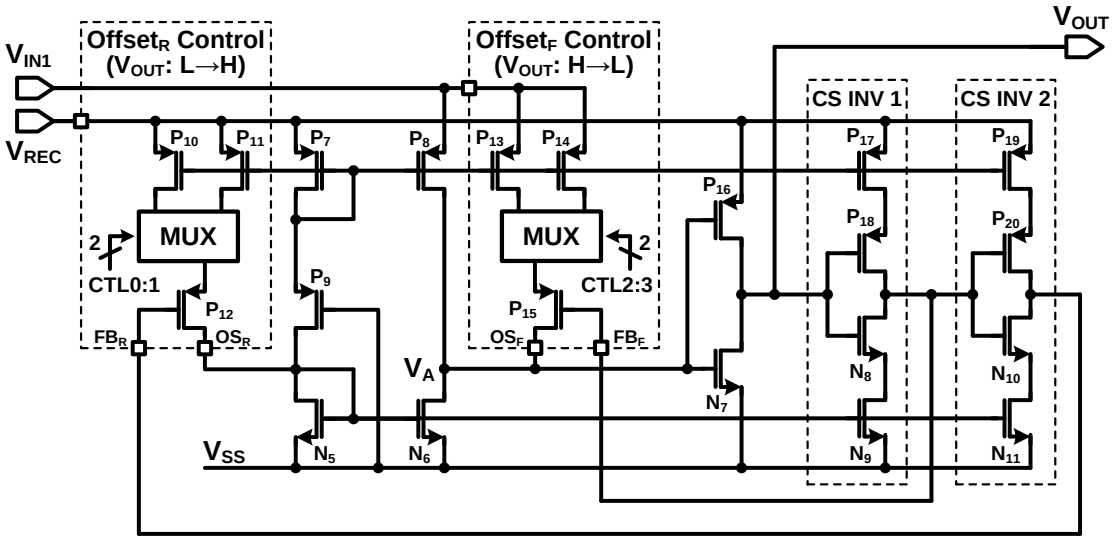
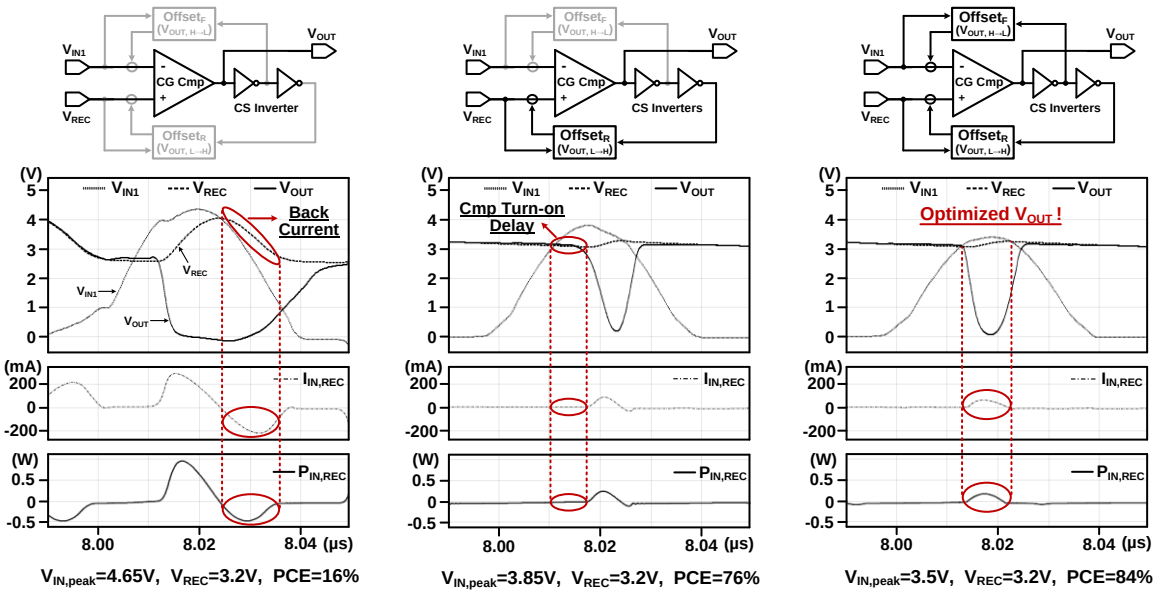


Fig. 2.6. Schematic diagram of the high speed comparator with two offset-control functions, $Offset_F$ for the V_{OUT} falling edge and $Offset_R$ for the V_{OUT} rising edge.

When $V_{IN1} > V_{REC}$, the current flowing through P_8 becomes larger than that of P_7. Then, the gate voltage of the output inverter, V_A, rapidly increases, and V_{OUT} falls to turn P_1 on. The $Offset_F$ and $Offset_R$ blocks are implemented by using current sources, P_{13}-P_{14} and P_{10}-P_{11}, within the comparator, MUXs, and the control switches, P_{15} and P_{12}. These blocks inject offset currents to the comparator inputs alternatively, inducing the desired timing. For example, when V_{OUT} is high, P_{15} turns on, and an offset current flows into the comparator positive input branch (V_{REC}) through OS_F, causing V_A to increase. Therefore, V_{OUT} starts to fall earlier before V_{IN1} exceeds V_{REC}. The offset current is programmable by using 2-bit off-chip control signals per offset-control block, CTL0:1 and CTL2:3, in order to adjust the rectifier timing in response to process variations.

2.2.4. Effects of Offset-Control Functions on PCE

Simulation results depicting the relationship between the PCE and offset-control functions are shown in Fig. 2.7. To understand the effects of the offset-control functions better, we have overlapped the rectifier input/output voltages, input current, and input power waveforms while adjusting V_{IN} amplitude to achieve a constant V_{REC} = 3.2 V for R_L = 500 Ω.



(a) (b) (c)

Fig. 2.7. Simulation results of the active rectifier showing waveforms of the input/output voltages, input current, and input power with V_{REC} = 3.2 V and R_L = 500 Ω, (a) without any offset-control function, (b) with only Offset_R function, and (c) with both Offset_F and Offset_R functions.

Fig. 2.7a shows that with no comparator offset-control function in place, the back current resulting from the turn-off delay severely degrades the PCE. This back current can be prevented by using the Offset_R function, as shown in Fig. 2.7b. Even though Offset_R improves the PCE significantly, the input power to the rectifier is still being reduced due to the comparators' turn-on delay, T_{PHL}. Therefore, there is room to further improve the rectifier PCE as well as voltage conversion efficiency (VCE) by using both Offset_F and Offset_R functions to compensate for T_{PHL} and T_{PLH} delays, respectively. Fig. 2.7c clearly shows that with both functions in place V_{OUT} transitions happen at the right times, and the PCE is maximized.

Since the offset-control blocks consume additional power to provide the offset currents, the power overhead for employing these functions needs to be considered. Fig. 2.8 shows the simulated comparator power consumption vs. V_{REC} and its break down between the two blocks.

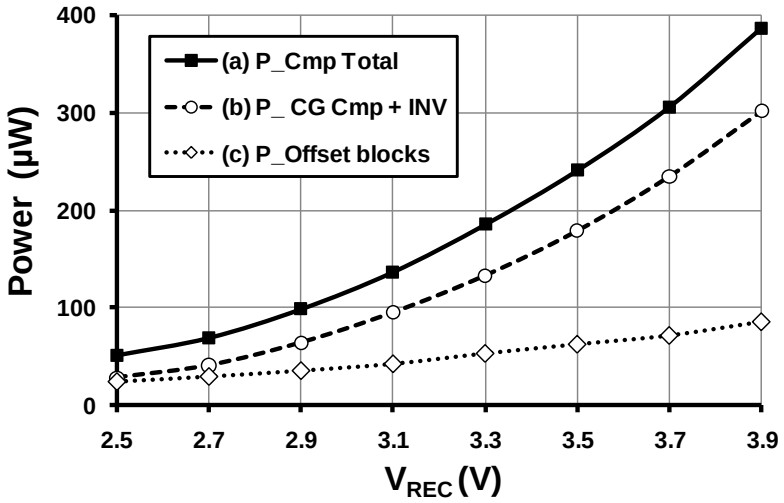


Fig. 2.8. Simulated power consumption of the comparator vs. V_{REC} showing power overheads for employing the offset-control functions (f_c = 13.56 MHz, R_L = 500 Ω, and C_L = 10 μF).

When V_{REC} increases, the power consumption of the CG comparator, curve-(b) also increases, contributing a large portion of the comparator power consumption, curve-(a). This is because both the static current of the CG comparator and the shoot-through current of the output inverter increase with V_{REC}. Moreover, since the comparator offsets have been tuned for V_{REC} = 3.12 V, power consumption becomes more severe at higher V_{REC}. On the other hand, curve-(c), the offset-control blocks' power consumption shows a mild increase when V_{REC} increases. It is because the offset- control blocks consume only dynamic power for a short period. For V_{REC} = 3.12 V, the entire high speed comparator consumes 135 μW, 40 μW of which is the power consumption of the offset-control blocks. The entire comparator power consumption is little affected by the load conditions as long as V_{REC} is fixed.

Since no supply voltage is available before the active rectifier starts its operation, it is necessary for the rectifier to have self-startup capability. Our high speed comparator, shown in Fig. 2.6, has a common-gate input stage, in which the two comparator input voltages, V_{IN1} and V_{REC}, are also the positive supply voltages. Hence the rectifier sinusoidal input voltage, $V_{IN1,2}$, guarantees that the rectifier reliably starts up even before V_{REC} is sufficiently charged up.

2.2.5. Measurement Results

The active rectifier was fabricated in the ON Semiconductor 0.5-μm 3M2P standard CMOS process (minimum transistor length of 0.6 μm) for its relatively high voltage handling capability. Fig. 2.9 shows the chip micrograph, which includes the active rectifier, overvoltage protection circuit, and the low dropout regulator, occupying 0.4 mm^2 of the Si area with $W_p / L_p = W_n / L_n$ = 2100 μm / 0.6 μm.

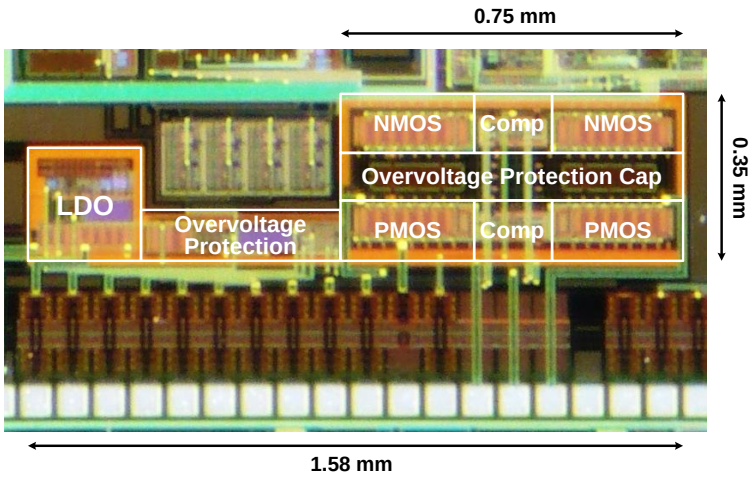


Fig. 2.9. Fabricated chip micrograph and its floor plan, including the active rectifier, overvoltage protection circuit, and low dropout regulator.

Fig. 2.10 shows the lumped model of the circuit used in the rectifier measurements with emphasis on the inductive and capacitive parasitic components, which combined with the measurement instrument (oscilloscope) parasitic, cause distortion in the measured waveforms at this relatively high operating frequency (f_c = 13.56 MHz). For instance, when the rectifier starts conducting, there is a sudden drop in V_{IN1} - V_{IN2}, and when it stops conducting, the stored energy in the interconnect inductors cause a sudden voltage hike across the rectifier inputs. Therefore, it is important to note that the voltages measured across the coil or load, V_{XY}, are not exactly the same as those measured on the rectifier packaged IC pins, V_{XY}^* (LQFP176). For example, L_{bond}, the parasitic inductance of the wirebond, and L_{wire}, the parasitic inductance of the external interconnects, cause the rectifier input voltage at the package, V_{IN1}^* - V_{IN2}^*, to be distorted

and have a peak voltage higher than the sinusoidal input voltages at the secondary coil, V_{IN1} - V_{IN2}.

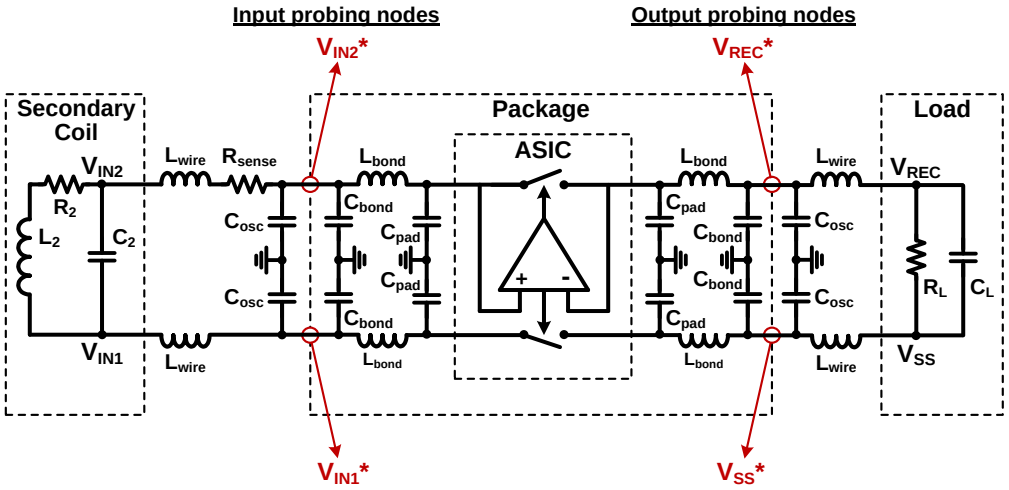


Fig. 2.10. Lumped model of the circuit used in active rectifier simulations, showing capacitive and inductive parasitic components of the wire-bond and external interconnects.

Moreover, the instantaneous input current flows into the rectifier through the parasitic inductors only during the rectifier turn-on, which is much shorter than one operating cycle (see Fig. 2.7c). Therefore, the frequency components, which affect the parasitic inductors and distort the voltage waveforms, are effectively much higher than the carrier frequency at 13.56 MHz. Unfortunately, this effect has not been considered in the recent literature on active rectifiers, and consequently, depending on how the measurements are done, the reported results on the rectifier efficiency might have been optimistic.

Fig. 2.11 shows the active rectifier measured input and output voltage waveforms. In these measurements we refrained from directly probing V_{OUT} because it could load and affect the comparator performance. Instead, C_L was reduced from 10 μF to 100 pF to better show the effects of offset-control functions. For all measurements and simulations in this section, we enabled the Offset_R to prevent the back currents. When the Offset_F function was enabled, V_{REC} started to increase ~5 ns earlier than without Offset_F. This comparison, which is consistent with the simulation results in Fig. 2.7, shows that the

comparators turn the rectifier on faster to deliver current for a longer time period. Therefore, the Offset_F function not only improves the PCE but also reduces the rectifier dropout voltage, V_{drop}, which is defined as the difference between $V_{IN1,peak}^{*}$ and V_{REC}. There is also a small phase shift between the ripple on V_{REC} and $V_{IN1,2}^{*}$ due to the parasitic components.

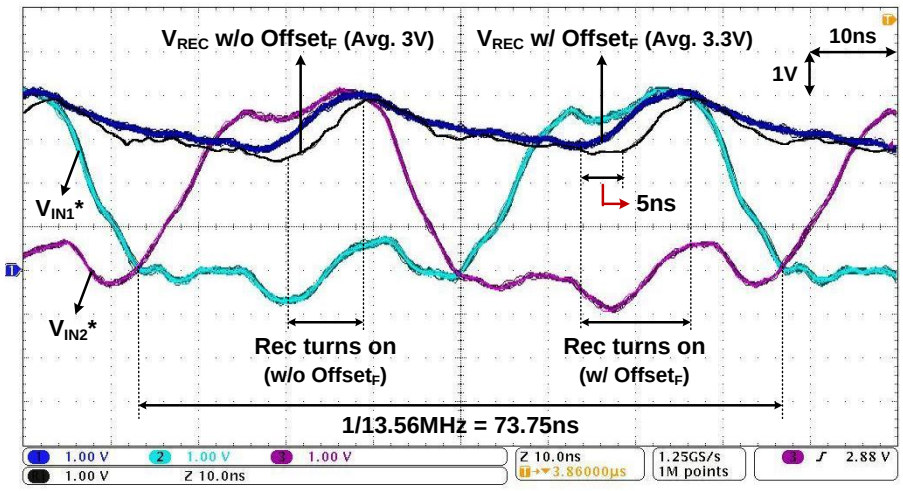


Fig. 2.11. Measured waveforms of the input and output voltages of the rectifier with and without the Offset_F function (f_c = 13.56 MHz, $V_{IN,\,peak}$ = 4.1 V, R_L = 500 Ω, and C_L = 100 pF).

We measured the PCE and V_{drop} by sweeping 1) V_{REC}, 2) R_L connected directly across the rectifier, substituting the regulator, and 3) f_c. In order to measure the rectifier input current, we connected a small resistor, R_{sense} = 10 Ω, in series with the rectifier input as a current sensor and differentially measured the voltage across it. The rectifier input power was calculated by integrating the instantaneous product of the input current and voltage samples. The output power for the PCE was obtained by measuring the $V_{REC,RMS}$. The peak input voltage, $V_{IN,peak}$, can be expressed as the sum of V_{REC} and V_{drop}.

Fig. 2.12 shows the measured and simulated PCE and V_{drop} vs. V_{REC} with C_L = 10 µF, R_L = 500 Ω, and f_c = 13.56 MHz. All simulated results in this section are post-layout and include the estimated parasitic components of the LQFP176 package (see Fig. 2.10). Fig. 2.12a shows that for V_{REC} = 3.12 V, the maximum PCE with both offset-control functions was measured to be 80.2% (curve-b), which was slightly lower than the

maximum post-layout simulated PCE of 84.5% (curve-a) and schematic simulated PCE of 87% due to the effects of parasitics and the current sensing resistor. The measured PCE without Offset_F (curve-c) is ~10% lower than the PCE with Offset_F. When V_{REC} was higher or lower than 3.12 V, the PCE gradually decreased because the comparator offsets were only adjusted for V_{REC} = 3.1 ~ 3.2 V. For other V_{REC} values, the comparator offsets can be easily readjusted using CTL0:3 in Fig. 2.2.

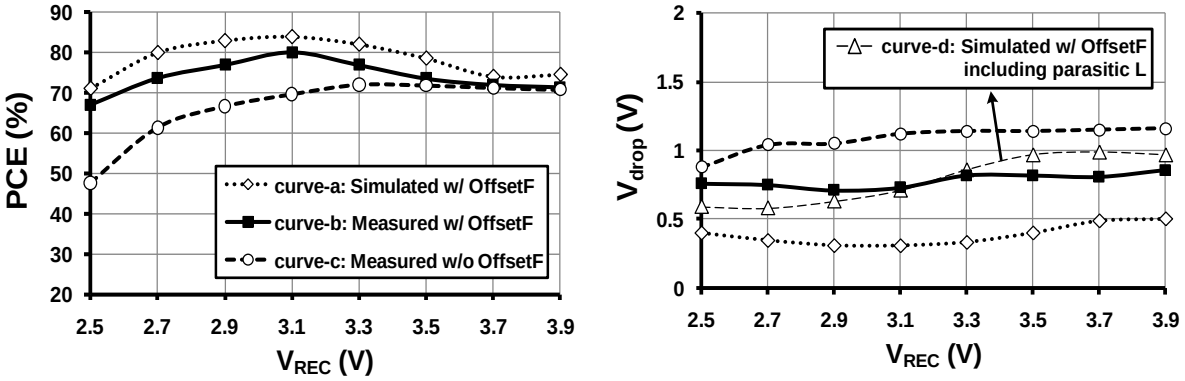
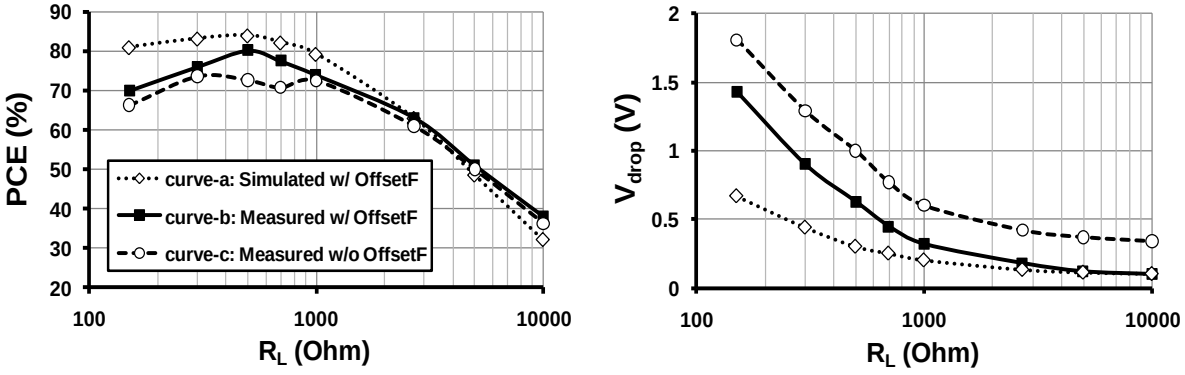


Fig. 2.12. Measured and simulated (a) PCE and (b) V_{drop} vs. V_{REC} when R_L = 500 Ω, C_L = 10 μF, and f_c = 13.56 MHz.

In Fig 2.12b, the measured V_{drop} with Offset_F (curve-b) shows 0.7 V dropout, which is 0.4 V higher than the simulated V_{drop} with Offset_F (curve-a). This is due to the interconnect inductances increasing $V_{IN1,peak}^*$ as explained earlier. For example, $V_{IN1,peak}^*$ was measured ~250 mV higher than $V_{IN1,peak}$ in Fig 2.10 after shorting R_{sense}. By including these parasitic inductors in our simulations (L_{bond} + L_{wire} = 25 nH), we were able to verify the cause of V_{drop} variations by producing results (curve-d) that were closer to the measured V_{drop} (curve-b). V_{drop} is also affected by the output current, I_{REC}, and PCE. In Fig. 2.12b, a higher V_{REC} with fixed R_L requires higher I_{REC} through the rectifier, which generates a larger voltage drop across the rectifying transistors, increasing V_{drop}. Furthermore, a rectifier with lower PCE requires more current from the coil to reach a certain V_{REC}, which also increases V_{drop}. Overall, measured and simulated results clearly showed that V_{drop} is reduced by using both offset-control functions.

Fig. 2.13a shows the measured and simulated PCE vs. R_L with C_L = 10 µF, V_{REC} = 3.12 V, and f_c = 13.56 MHz. As R_L increases, the rectifier output power for the same V_{REC} decreases. Therefore, the rectifier internal power dissipation for switch losses, $P_{Loss,total}$, and comparators, $P_{Comparator}$, become more significant in (4) and reduce the PCE. The measured and simulated V_{drop} vs. R_L in Fig. 2.13b shows that V_{drop} decreases by increasing R_L. It is because larger R_L requires smaller I_{REC}, leading to smaller voltage drop across the rectifying transistors.



(a) (b)

Fig. 2.13. Measured and simulated (a) PCE and (b) V_{drop} vs. R_L with V_{REC} = 3.12V, C_L = 10 µF, and f_c = 13.56 MHz.

Fig. 2.14a shows the measured and simulated PCE vs. f_c with C_L = 10 µF, V_{REC} = 3.12 V, and R_L = 500 Ω. The transistor dimensions and comparator offsets of our rectifier were optimized for operating at 13.56 MHz. Therefore, the PCE decreases at higher frequencies due to the comparator delays. At lower frequencies, the PCE also decreases a little bit since the fixed comparator offset turns off the rectifier earlier. Fig. 2.14b shows the measured and simulated V_{drop} vs. f_c. Even though I_{REC} is fixed in these experiments, the PCE variation by frequency also affects V_{drop}. Therefore, lower PCE at higher frequencies leads to higher V_{drop}.

Table 2.1 shows the full-wave rectifier benchmarking table, comparing our work with previously reported rectifiers. It can be seen that despite its relatively large feature length process and size, the active rectifier reported here, to the best of our knowledge,

provides the highest measured PCE = 80.2% ever reported at 13.56 MHz, thanks to its high speed comparators that are equipped with offset-control functions for both rising and falling edges. With an input peak voltage of 3.8 V, this rectifier can deliver more than 20 mW at V_{REC} = 3.12 V, which is required for high power IMDs such as the implantable multichannel wireless neural recording and stimulating system that is being developed in GT-Bionics lab [65]. By shortening the connection between L_2 and the rectifier input port when they are both embedded in an IMD and thus reducing the parasitic components shown in Fig. 2.10, we expect the rectifier PCE to move closer to the simulated level of 87%. Further, migrating to a smaller feature length process is expected to further improve the PCE and bandwidth by lowering the threshold voltages and comparator delays. Table 2.2 summarizes some additional specifications of the active rectifier.

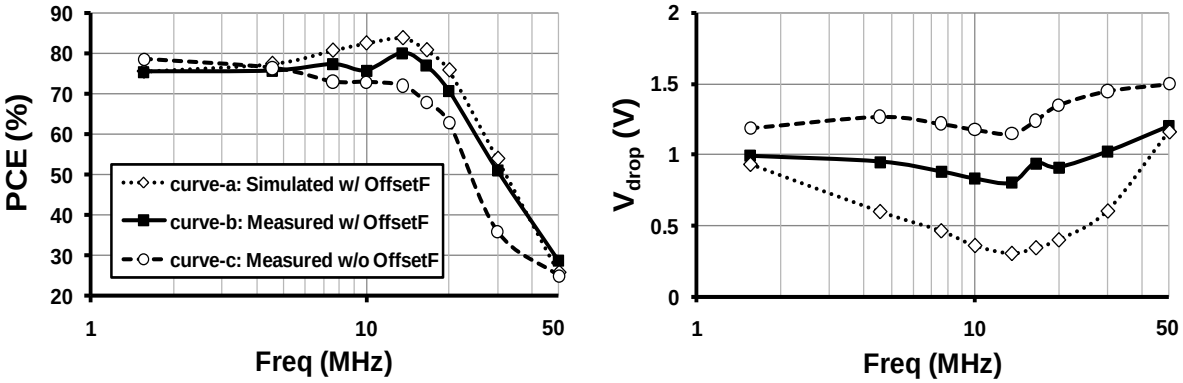


Fig. 2.14. Measured and simulated (a) PCE and (b) V_{drop} vs. f_c with V_{REC} = 3.12V, C_L = 10 µF, and R_L = 500 Ω.

Table 2.1: Full-wave rectifier benchmarking

Publication		2006 [29]	2007 [22]	2008 [30]	2009 [27]	2009 [32]	2009 [31]	**This work**
Technology		0.35 µm CMOS	0.5 µm Schottky	0.5 µm CMOS	0.18 µm CMOS	0.18 µm CMOS	0.35 µm CMOS	**0.5 µm CMOS**
$V_{IN,\,peak}$ (V)		3.5	5	5	0.8	1.25	2.4	**3.8**
V_{REC} (V)		3.22	4.2	4.36	1.8	0.96	2.08	**3.12**
R_L (kΩ)		1.8	2.8	1	270	2	0.1	**0.5**
f_c (MHz)		13.56	4	0.1~2	13.56	10	0.2~1.5	**13.56**
Area (mm^2)		0.0055	N/A	0.4	0.83	0.86	0.4	**0.18**
PCE (%)	Sim.	87	N/A	90.4	N/A	N/A	87	**87**
	Meas.	N/A	75	84.8	54.9	76	N/A	**80.2**

Table 2.2: Additional active rectifier specifications

V_{ThN} / V_{ThP}	0.78 V / 0.92 V
Nominal rectifier output power	20 mW
Minimum rectifier input voltage	3.2 V (2.9 V*)
Ripple rejection capacitor (C_L)	10 μF (ESR = 80 mΩ)
Output ripple	80 mV_{pp}
Comparator power consumption	135 μW*
Comparator turn-on delay with $Offset_F$	0.75 ~ 1.5 ns*
Comparator turn-off delay with $Offset_R$	-0.7 ~ 0.5 ns*
Primary coil diameter / inductance (L_1)	16.8 cm / 0.88 μH
Secondary coil diameter / inductance (L_2)	3.0 cm / 0.41 μH
Size of rectifying switches ($W_p / L_p = W_n / L_n$)	2100 μm / 0.6 μm
Total area on chip	0.4 mm^2

*From simulation

2.3. Active Voltage Doubler

2.3.1. Active Voltage Doubler Architecture

Fig. 2.15 shows the topology of the conventional passive voltage doubler using either diodes or diode-connected transistors. It consists of one capacitor, C_{IN}, and two diodes, D_N and D_P, with forward dropout voltages of V_{DN} and V_{DP}, respectively. Rectified output voltage, V_{OUT}, is low pass filtered by C_L, and supplies the load resistor, R_L. The sinusoidal input voltage, V_{IN}, generated across the secondary resonance circuit, L_2C_2, has a peak amplitude of $V_{IN,peak}$.

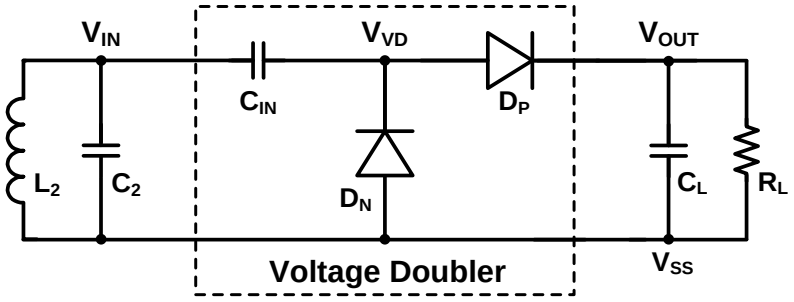


Fig. 2.15. Schematic diagram of the passive voltage doubler using diodes or diode-connected transistors.

In the passive voltage doubler, V_{OUT} can reach a maximum voltage of $2V_{IN,peak}$ - V_{DN} - V_{DP} because of the dropout voltage across D_N and D_P. The total dropout voltage of the voltage doubler, V_{Drop}, can be calculated from,

$$V_{Drop} = 2V_{IN,peak} - V_{OUT} = V_{DN} + V_{DP.} \quad (2.4)$$

This equation shows that the diode dropout voltages, V_{DN} and V_{DP}, directly affect the voltage doubler output voltage and consequently its PCE. Thus, substituting them with fast MOS switches with low on-resistance and leakage would be an effective way of reducing V_{Drop} and improving the PCE.

Fig. 2.16 shows a simplified schematic diagram of the proposed active voltage doubler, in which two pass transistor switches, N_1 and P_1, are driven by high-speed comparators, CMP_N and CMP_P, respectively. When $V_{VD} < V_{SS}$, CMP_N output goes high, N_1 turns on with a low dropout voltage, $V_{DS(N1)}$, and C_{IN} is charged to $V_{IN,peak}$ - $V_{DS(N1)}$ in the shown polarity. Similarly, when $V_{VD} > V_{OUT}$, CMP_P output goes low, P_1 turns on with a low dropout voltage, $V_{SD(P1)}$, and current flows through P_1 to charge R_LC_L in the shown polarity. Therefore, after a few cycles, V_{OUT} is charged up to $2V_{IN,peak}$ - $V_{DS(N1)}$ - $V_{SD(P1)}$, and the total dropout voltage, V_{Drop} = $V_{DS(N1)}$ + $V_{SD(P1)}$, which results from the instantaneous input current flowing through the on-resistance of N_1 and P_1, will be much smaller than that of the passive voltage doubler in Fig. 2.15 ($V_{GS(N)} + V_{SG(P)}$).

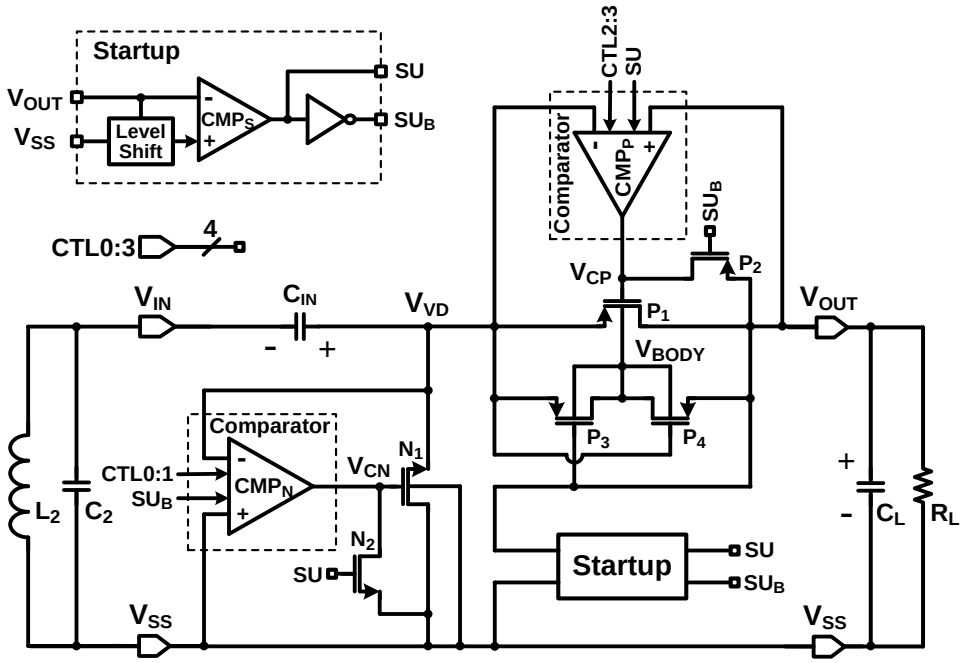


Fig. 2.16. Schematic diagram of the proposed active voltage doubler employing high speed offset-controlled comparators, CMP_N and CMP_P, to drive N_1 and P_1 pass transistors, respectively, for high PCE.

To drive N_1 and P_1 at high frequencies in the order of 13.56 MHz, comparators are equipped with internal offset-control functions that are externally adjustable (CTL0:3) to reduce the effects of the comparators' delay. We have also adopted the dynamic body biasing technique from [18] with auxiliary transistors, P_3 and P_4, automatically connecting V_{BODY} to the highest potential between V_{VD} and V_{OUT}.

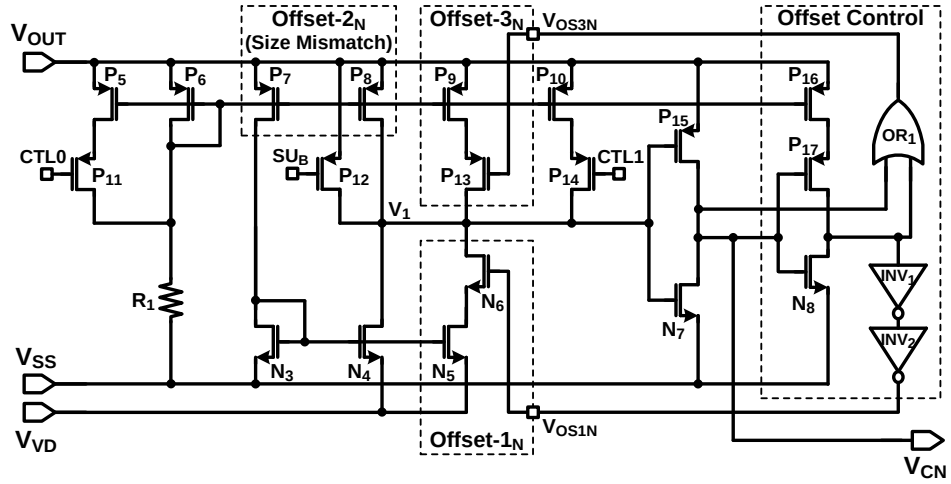
Since the comparators are supplied from V_{OUT}, which is initially at 0 V, it is necessary for the active voltage doubler to have startup capability. The startup block in Fig. 2.16, which has been described in next section, generates a complementary pair of startup enable signals, *SU* and SU_B, depending on the V_{OUT} level to control the startup switches, N_2 and P_2, as well as the comparators. When V_{OUT} is too low to operate the comparators, the startup circuit sets *SU* = high and SU_B = low, which turn on N_2 and P_2, respectively, while disabling the comparators. In this condition, both N_1 and P_1 are diode-connected to form a passive voltage doubler, which starts charging V_{OUT} regardless of the comparators' status. When V_{OUT} exceeds a certain level that is sufficient to operate the comparators, *SU* and SU_B toggle and turn N_2 and P_2 off, while enabling the comparators to normally run the active voltage doubler.

2.3.2. Circuit Details and Design Considerations

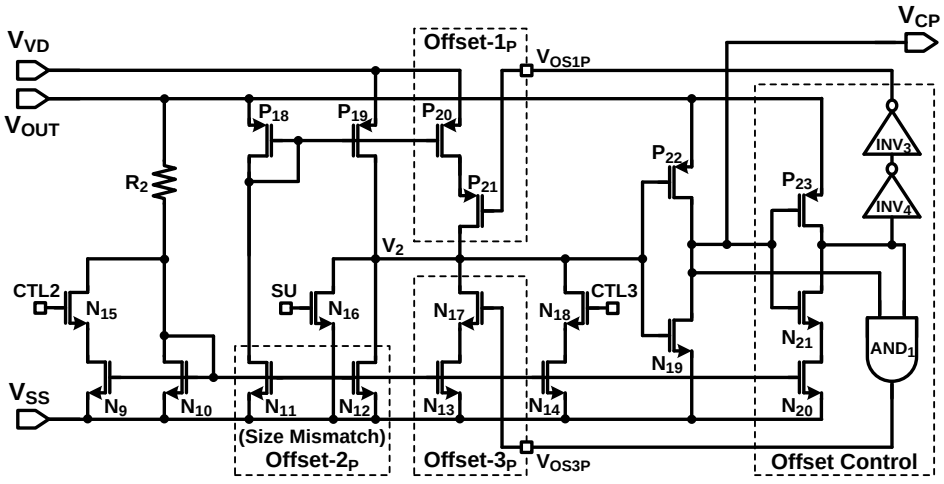
CMP_N and CMP_P need to drive large gate capacitances of N_1 and P_1 at high frequencies, respectively. Thus, key design parameters are drive capability and short delay. Comparator delay can reduce the PCE by either decreasing the input power that could otherwise be delivered to the load or allowing instantaneous back currents that flow from C_L back to L_2C_2 tank when $V_{IN} < V_{OUT}$. To reduce such delays, we have designed improved high-speed comparators with adjustable internal offsets, which basic concept was introduced in section 2.2.3. These built-in offset control functions help comparators turn their pass transistors on and off at proper times, leading to higher PCE.

Fig. 2.17 shows the schematic diagram of two symmetrical high-speed

comparators, CMP_N in Fig. 2.17a and CMP_P in Fig. 2.17b, each of which is equipped with three built-in offset-control functions. In Fig. 2.17a, P_7-P_8, N_3-N_4, and P_{15}-N_7 form a common-gate comparator, which input terminals at the sources of N_3 and N_4 are connected to V_{SS} and V_{VD}, respectively. P_6 and R_1 form a biasing branch, which is mirrored on to P_7 and P_8. Since the gate of the diode-connected N_3 is coupled with N_4, currents flowing through N_3 and N_4 depend on their source voltages, V_{SS} and V_{VD}, respectively. When $V_{VD} < V_{SS}$, the current flowing through N_4 tends to be larger than that of N_3, P_7, and P_8. Hence, V_1, the input of the P_{15}-N_7 inverter rapidly drops, leading to a high comparator output voltage, V_{CN}, which turns N_1 on.



(a)



(b)

Fig. 2.17. Schematic diagram showing three offset-control functions in high speed comparators, (a) CMP_N and (b) CMP_P: Offset-1 for turn-on delay, Offset-2 for turn-off delay, and Offset-3 for reliable turn-off.

Even though common-gate comparators are considered high speed due to their low input impedance and simple structure, their speed of operation in our 0.5-µm process was not fast enough to drive large capacitive loads (N_1 and P_1) at 13.56 MHz. Therefore, we added Offset-1_N and Offset-2_N inside CMP_N (and their duals in CMP_P) in order to compensate for the turn-on and turn-off delays, respectively. Offset-1_N block is implemented using N_5 current source, controlled by N_6 switch, which can pull additional offset current from CMP_N output branch, leading V_1 to start dropping earlier when this offset mechanism is activated by V_{OS1N} = high. Constant Offset-2_N has been implemented using the size mismatch between P_8 and P_7. The larger W/L ratio of P_8 pushes additional offset current into the comparator output branch to increase V_1 early.

The offset control signal, V_{OS1N}, is provided by an offset control block that consists of the current-starved inverter, P_{16}-P_{17}-N_8, and other logic gates in Fig. 2.17a. When $V_{VD} > V_{SS}$, V_{CN} = low, and V_{OS1N} = high. Thus, N_6 turns N_5 on to pull offset current in parallel with N_4 at a level that is higher than the additional current that is pushed in P_8 by Offset-2_N. Therefore, V_{CN} starts to increase earlier to turn on N_1 a bit before V_{VD} falls below V_{SS} to compensate for the comparator turn-on delay. Once V_{CN} = high, the Offset-1_N block turns off, and the offset current pushing through P_8 becomes dominant. As a result, V_{CN} starts to decrease earlier to turn N_1 off a bit before V_{VD} exceeds V_{SS} to compensate for the comparator turn-on delay. In this case, V_{OS1N} goes high after the delay generated by the current- starved inverter, which should be shorter than one carrier cycle period. Since V_{OS1N} switches to high when V_{VD} is much higher than V_{SS}, it does not cause any fluctuation or instability issues through its feedback loop.

Sudden variations in V_{VD} may occur with rapid changes in the forward current due to interconnect parasitic inductance between L_2C_2 tank and the voltage doubler. These variations may disrupt proper switching of the pass transistors and should be avoided. To protect the comparators against such effects, we have added a 3rd offset branch, Offset-3_N, which consists of P_9 current source, controlled by P_{13} switch. When V_{CN} goes low, it

takes a while before the current-starved inverter output goes high. During this time, V_{OS3N} = low, activating the Offset-3_N branch to inject additional current into V_1 node and prevent V_{CN} from undesired changes due to V_{VD} variations. This will keep N_1 off until the next carrier cycle. It should be noted that the current-starved inverter delay does not need to be accurate, and its changes due to process variations can be tolerated as long as the delay time is terminated before the next transition time.

In addition, we have added 4-bit off-chip digital control signals, two for each comparator, CTL0:1 (CMP_N) and CTL2:3 (CMP_P), which should be connected to either V_{OUT} (high) or V_{SS} (low), to adjust the switching times of the voltage doubler against process variations before the chip is used. For example, when CTL0 = low, the reduced current in P_8 drives node V_1 more weakly, delaying V_{CN} decrement and the onset of turning N_1 off. On the contrary, when CTL1 = low, P_{10} increases the size mismatch in the Offset-2_N, V_{CN} increases more rapidly, and N_1 turns off earlier. Moreover, startup control switches, P_{12} and N_{16}, are added in CMP_N and CMP_P, respectively, for a reliable startup operation as a passive voltage doubler. These switches turn on during the initial startup period and ensure that V_{CN} and V_{CP} are connected to V_{SS} and V_{OUT}, respectively.

The active voltage doubler is cable of starting up before its supply rail, V_{OUT}, is charged up to the level that is needed for the comparators to operate. The startup circuit in Fig. 2.18 reconfigures the doubler circuit as a diode-connected passive voltage doubler by generating SU and SU_B signals based on V_{OUT}. When V_{OUT} = 0 V, comparator outputs, V_{CN} and V_{CP} in Fig. 2.16, are also at 0 V. In this condition, P_1 and N_1 are diode-connected and conduct when $V_{VD} > V_{Th(P1)}$ and $V_{VD} < -V_{Th(N1)}$, respectively, and V_{OUT} starts to charge up. In Fig. 2.18, when $V_{OUT} < V_{Th(N22)} + V_{Th(P24)}$, P_{24} stays off and V_3 remains at 0 V through R_4. SU and SU_B follow V_{OUT} and V_{SS} and result in N_1 and P_1 to stay diode-connected. During the same period, P_{12} and N_{16} in Figs. 2.17a and 2.17b force V_{CN} and V_{CP} to be low and high, respectively, further supporting N_1 and P_1 to be diode- connected. When $V_{OUT} > V_{Th(N22)} + V_{Th(P24)}$, N_{22} turns on creating sufficient voltage across R_3 to turn

on P_{24} and pull V_3 up. This, SU and SU_B become V_{SS} and V_{OUT}, respectively, turning N_2 and P_2 off, releasing the comparator outputs, and allowing N_1 and P_1 to operate as switches. Both R_3 and R_4 have 1 MΩ values to reduce static power consumption.

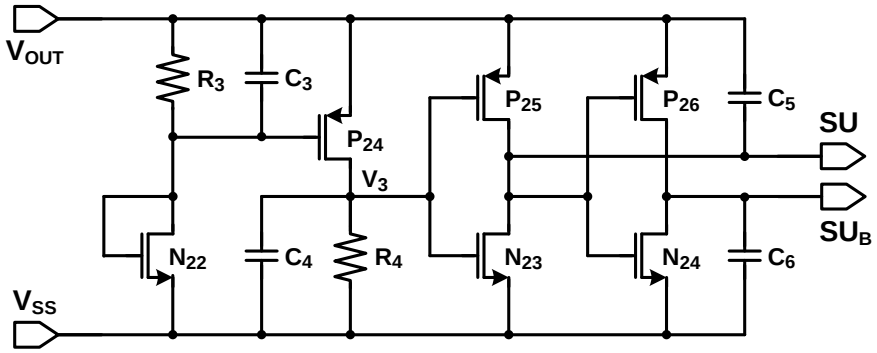


Fig. 2.18. Schematic diagram of the startup circuit, which generates the startup enable signals, SU and SU_B.

Fig. 2.19 shows the simulated waveforms for the self-startup process of the active voltage doubler, which guarantees that V_{OUT} is charged up to about 1.4 V before resuming its normal operation. Since sub-threshold operation of transistors also conducts a small amount of currents, the startup switching voltage may practically be less than the theoretical limit of $V_{Th(N22)} + V_{Th(P24)}$.

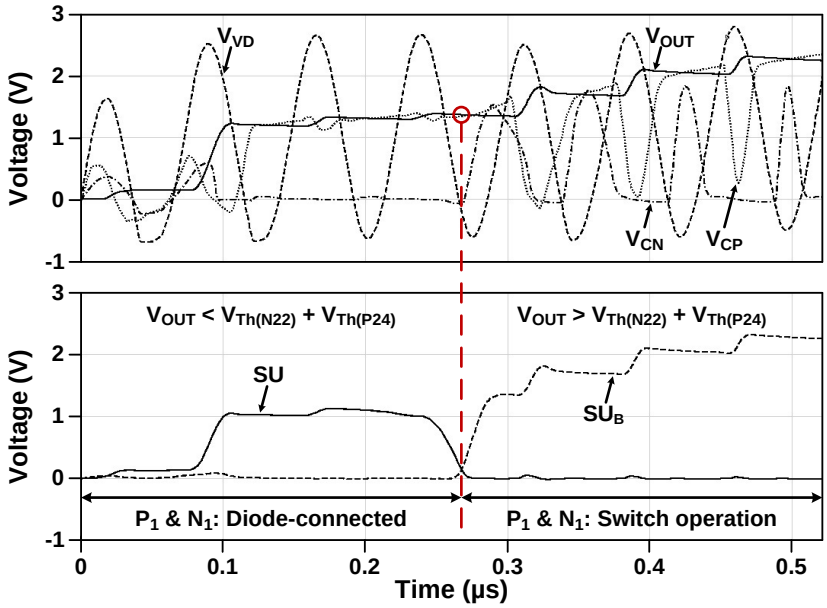


Fig. 2.19. Simulation results showing self-startup capability of the active voltage doubler ($V_{IN,peak}$ = 1.5 V, V_{OUT} = 2.4 V, R_L = 1kΩ, C_{IN} = C_L = 1 nF, and f_c = 13.56 MHz).

2.3.3. PCE Optimization with Triple Offset-control Functions

The PCE of the active voltage doubler can be expressed as,

$$\text{PCE} = \frac{P_{OUT}}{P_{IN}} = \frac{P_{Load}}{P_{Load} + P_{CMP} + P_{Tr,sw} + P_{Tr,Ron}} \tag{2.5}$$

where P_{Load} is the power delivered to the load and P_{CMP} is the internal power consumption of comparators excluding the power needed to drive the gates of P_1 and N_1. $P_{Tr.sw}$ and $P_{Tr.Ron}$ are the power losses in the pass transistors due to gate switching and dissipation in R_{on}, respectively. The sizing of P_1 and N_1 plays an important role in the PCE optimization since $P_{Tr.sw}$ and $P_{Tr.Ron}$ are affected by W and L of each pass transistor. Some of the terms in (2.5) can be approximated by,

$$P_{Load} = \frac{{V_{OUT}}^2}{R_L} \tag{2.6}$$

$$P_{Tr,sw} \approx W_p C_{gp} {V_{OUT}}^2 f_c + W_n C_{gn} {V_{OUT}}^2 f_c \tag{2.7}$$

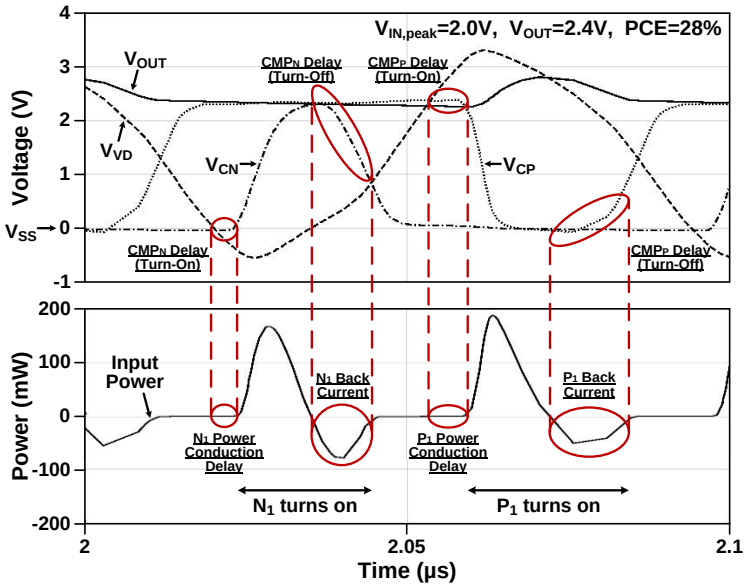
$$P_{Tr,Ron} \approx {I_p}^2 R_{onp} D + {I_n}^2 R_{onn} D = \frac{1}{D}\left(I_{Load} + I_{CMP} + I_{Tr,sw}\right)^2 \left(R_{onp} + R_{onn}\right)$$

$$= \frac{{V_{OUT}}^2}{D}\left(\frac{1}{R_L} + \frac{P_{CMP} + P_{Tr,sw}}{{V_{OUT}}^2}\right)^2 \left(R_{onp} + R_{onn}\right) \tag{2.8}$$

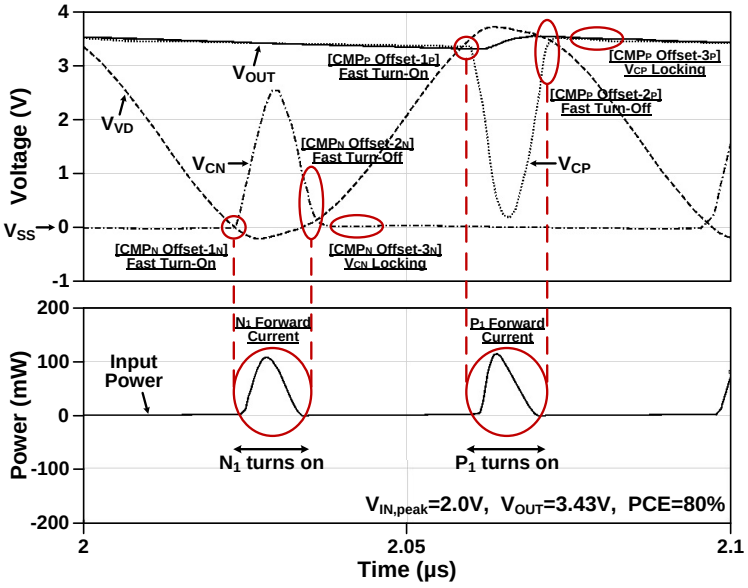
where W_p and W_n are the widths of P_1 and N_1, and C_{gp} and C_{gn} are the gate capacitance per unit width of P_1 and N_1, respectively. f_c = 13.56 MHz is the carrier frequency, and D is the operating duty cycle (see Appendix). I_p and I_n are currents flowing through P_1 and N_1, respectively, and they are assumed to be equal. We also found P_{CMP} at each V_{OUT} from simulations (0.1 ~ 0.8 mW), and used it in the PCE analysis. L_p and L_n are 0.6 μm, the minimum length in this process.

Even though larger widths of pass transistors decrease $P_{Tr.Ron}$, they increase switching losses, $P_{Tr.sw}$, due to larger parasitic gate capacitances. Hence, each pass transistor has an optimal size for minimum power dissipation depending on several parameters, such as V_{OUT}, R_L, and f_c. In Appendix, we have derived detailed equations for PCE and V_{Drop} while calculating optimal size of pass transistors for target specifications.

To further clarify the effects of offset-control functions on the PCE, in Fig. 2.20a and 2.20b we have compared simulation results that show the voltage doubler input/output voltages (V_{VD} and V_{OUT}), comparator output voltages (V_{CN} and V_{CP}), and input power waveforms with the offsets disabled and enabled, respectively.



(a)



Corner condition	FF	FS	SF	SS
V_{OUT} when $V_{IN,peak}$=2V	3.416V	3.421V	3.425V	3.42V
PCE	79.3%	79.6%	79.7%	79.6%

(b)

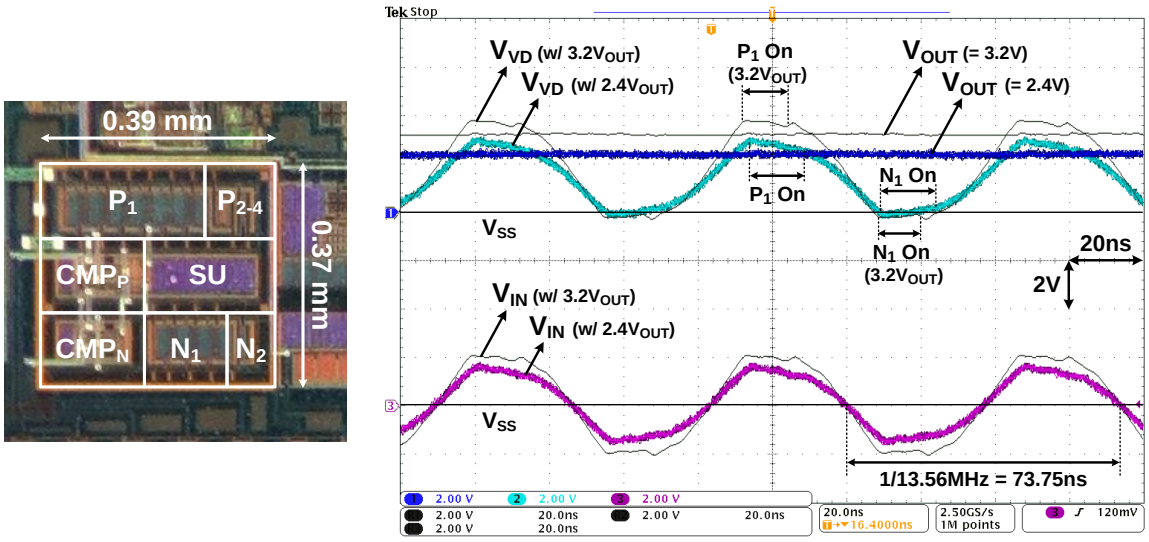
Fig. 2.20. Simulation results of the active voltage doubler showing waveforms of input/output voltages and input power with $V_{IN,peak}$ = 2 V, R_LC_L = *1* kΩ || *2* nF, C_{IN} = 2 nF, and f_c = 13.56 MHz, (a) without any offset-control functions, (b) with all three offset-control functions in nominal and process corner conditions.

In these simulations, we applied an AC voltage of $V_{IN,peak}$ = 2 V at f_c = 13.56 MHz to the input and connected R_LC_L = 1 kΩ || 2 nF to the output of the active voltage doubler. Fig. 2.20a shows that without offset-control functions, because of the comparator turn-on delays, V_{CN} and V_{CP} turn on N_1 and P_1 too late, respectively. This results in power conduction delays through the pass transistors, from L_2C_2 tank to the load, when $V_{VD} < V_{SS}$ or $V_{VD} > V_{OUT}$. Moreover, comparator turn-off delays result in V_{CN} and V_{CP} turning off N_1 and P_1 too late, inducing back currents flowing from C_{IN} to V_{SS} and from the output load to the L_2C_2 tank, respectively. Both of these effects significantly decrease V_{OUT} (= 2.4 V) and PCE (= 28%).

Fig. 2.20b shows that the abovementioned conduction delays and back currents can be significantly reduced using offset-control functions in comparators. Offset-1 and offset-2 functions compensate for the turn-on and turn-off delays, respectively, such that V_{CN} and V_{CP} can turn on/off their pass transistors at the right time, leading to the highest possible PCE. Thanks to these offset-control functions, the active voltage doubler can achieve much higher V_{OUT} (= 3.43 V) and PCE (= 80%) with the same $V_{IN,peak}$ and loading. Offset-3 function forces V_{CN} and V_{CP} to stay at V_{SS} and V_{OUT}, respectively, after their conduction periods in order to provide reliable pass transistor turn-off against spurious V_{VD} variations (not shown in these simulations).

2.3.4. Measurement Results

The active voltage doubler was fabricated in the ON Semiconductor 0.5-µm 3M2P standard CMOS process for its relatively high voltage handling capability. Fig. 2.21 shows the chip micrograph occupying 0.144 mm^2 area and the measured input and output waveforms of the active voltage doubler under two conditions when ($V_{IN,\,peak}$, V_{OUT}) = (1.46 V, 2.4 V) and (2 V, 3.2 V). Directly probing the comparator outputs induces extra loading, which results in undesired additional delays. Hence, we inferred the underlying events in the circuit by inspecting V_{IN} and $V_{VD} = V_{IN} + V_{Cin}$.



(a) (b)

Fig. 2.21. (a) Fabricated chip micrograph. (b) Measured waveforms of key nodes in the active voltage doubler, showing V_{IN}, V_{VD}, V_{OUT}, and V_{SS} for ($V_{IN,\,peak}$, V_{OUT}) = (1.46 V, 2.4 V) and (2 V, 3.2 V) when R_L = 1 kΩ, C_{IN} = C_L = 1 μF, and f_c = 13.56 MHz.

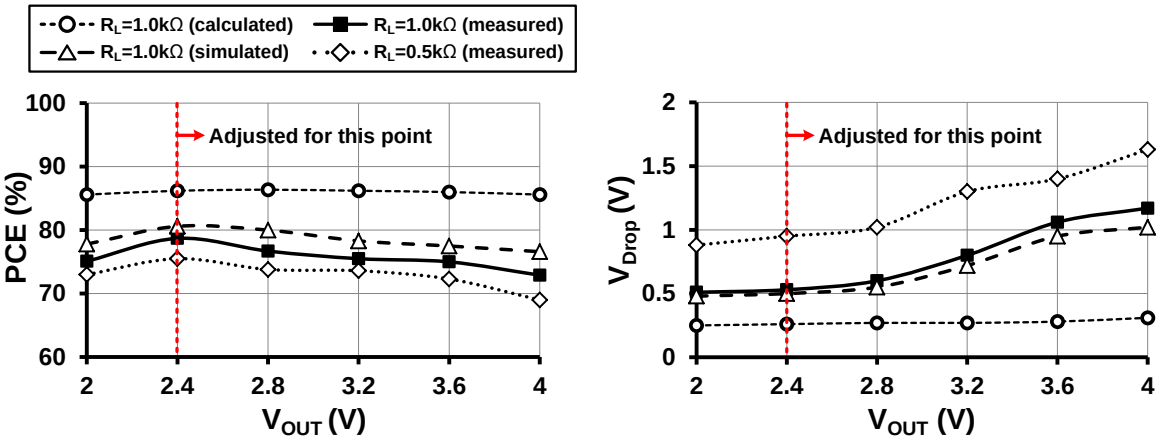
In Fig. 2.16, once V_{VD} exceeds V_{OUT}, P_1 turns on, and large current flows from the L_2C_2 tank to charge R_LC_L load. This forward flow creates a voltage drop across the parasitic coil resistance and the interconnect inductance, resulting in a small dip in V_{VD}. While P_1 is on, $V_{VD} = V_{OUT} + I_pR_{onp}$, which is fairly constant due to large C_L and L_2 that keep V_{OUT} and I_P constant, respectively. When P_1 turns off, the charging current instantaneously stops leading to a small bump in V_{VD} waveform following which V_{VD} returns to its normal sinusoidal shape. Therefore, P_1 and N_1 switching times can be estimated from V_{VD} variations, as shown in Fig. 2.21. We considered the peak voltages of V_{IN} and V_{VD} when P_1 and N_1 just turned on or off in order to measure $V_{IN.pp}$ (= $2V_{IN,peak}$) and $V_{VD,peak}$, respectively. In these measurements, R_L = 1 kΩ, C_{IN} = C_L = 1 μF, and f_c = 13.56 MHz.

To consider key factors that affect the active voltage doubler performance, we measured the PCE and V_{Drop} while sweeping 1) V_{OUT}, 2) R_L, and 3) f_c. Each panel in Fig. 2.22, 2.23, and 2.24 shows the calculated, simulated, and measured (in two conditions) values of the PCE and V_{Drop} to verify the accuracy of our measurements and circuit

models, while providing insight for improvements. Calculated PCE and V_{Drop} have been derived from (2.4) to (2.8) and the active voltage doubler model in the Appendix, where the switching times are assumed to be ideal.

Simulations are post-layout and include estimations of parasitic inductances. To measure the input current, we connected a small current-sense resistor, R_{sense} = 10 Ω, in series with the voltage doubler input and differentially measured the voltage across it. P_{IN} was then calculated offline by integrating the instantaneous product of the input current and voltage samples. V_{OUT} was also measured to calculate $P_{Load} = V_{OUT}^2/R_L$. We also considered $V_{Drop} = V_{IN,pp} - V_{OUT}$.

Fig. 2.22 shows the measured, simulated, and calculated PCE and V_{Drop} vs. V_{OUT} for R_L = 0.5 kΩ and 1 kΩ, $C_{IN} = C_L$ = 1 μF, and f_c = 13.56 MHz. In our measurements, the highest PCE was 79% achieved at V_{OUT} = 2.4 V, which was the onset of circuit operation with 1 kΩ loading.



(a) (b)

Fig. 2.22. Measured (a) PCE and (b) V_{Drop} vs. V_{OUT} with R_L = 0.5 and 1 kΩ, $C_{IN} = C_L$ = 1 μF, and f_c = 13.56 MHz.

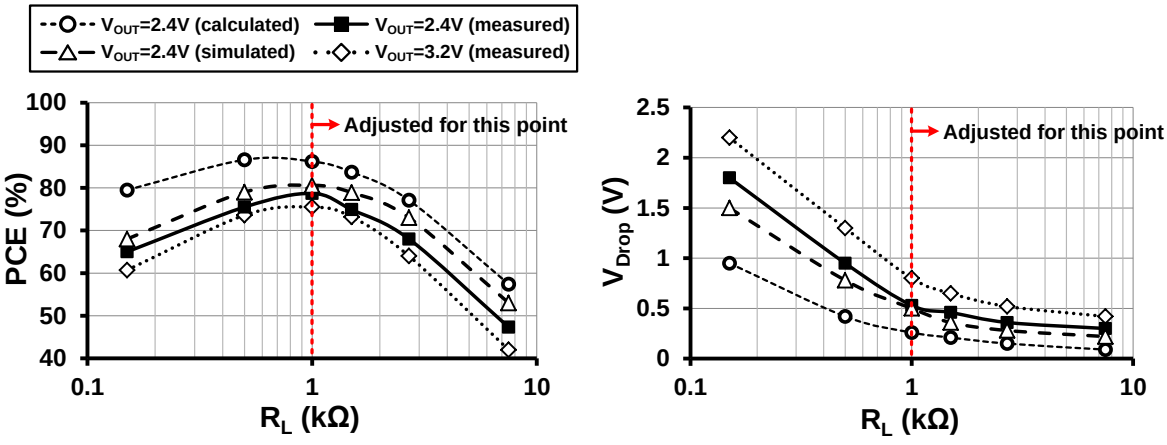
Unlike the active rectifier in which the dropout voltage stays more or less constant with the PCE generally improving with higher V_{OUT}, we observed increments in V_{Drop} and reductions in the PCE with increased V_{OUT}, which is evident in Fig. 2.22. These are some of the possible reasons behind this observation: First, increasing V_{OUT} with constant R_L

requires higher input current, resulting in higher power loss ($P_{Tr,Ron}$) in the pass transistors. The power dissipation of comparators (P_{CMP}) and gate switching ($P_{Tr,sw}$) also increase as the comparator supply voltage, V_{OUT}, increases. Second, it turned out that the 2-bit offset control that we have included in each comparator was only sufficient to adjust the switching times around V_{OUT} = 2 ~ 2.8 V. Therefore, the voltage doubler operation was not optimized for V_{OUT} > 2.8 V, resulting in both measured and simulated PCEs in Fig. 2.22a to degrade at higher V_{OUT}. It can be observed in Fig. 2.21b that P_1 and N_1 turn off too early when V_{OUT} = 3.2 V, limiting the input power delivered to the load and decreasing the PCE. Third, increasing V_{OUT} resulted in higher peaks on V_{IN} and V_{VD}, which were also noticeable in Fig. 2.21b, because of larger input current variations and more prominent effect of parasitic inductance. When $V_{VD} > V_{OUT} + V_{Th(P1)}$, P_1 is forced to conduct as a diode-connected transistor even after CMP_P tries to turn it off (due to suboptimal timing). This forced conduction in saturation region results in more power loss in P_1, and consequently lowers the PCE. Similarly, if $V_{VD} < V_{SS} - V_{PN\text{-}junction}$, it results in substrate leakage in N_1 because all NMOS body terminals should be connected to V_{SS} in this standard CMOS process. Therefore, some portion of the input current can flow through the parasitic PN junction instead of the N_1 switch, leading to additional power loss.

Calculated results in Fig. 2.22a and 2.22b show considerably higher PCE (86%) and lower V_{Drop} (0.27 V) compared to both simulated and measured results. Because in the theoretical circuit model we have assumed that the comparators turn the pass transistors on/off sharply with ideal timing regardless of variations in V_{OUT}, R_L, and f_c to achieve the maximum possible PCE, while the switching times in simulations and measurements are optimized for a certain operating condition, V_{OUT} = 2.4 V, R_L = 1 kΩ, and f_c = 13.56 MHz.

Fig. 2.23 shows the measured, simulated, and calculated PCE and V_{Drop} vs. R_L. In Fig. 2.23a, the maximum PCE was achieved with the designated R_L = 1 kΩ. As R_L

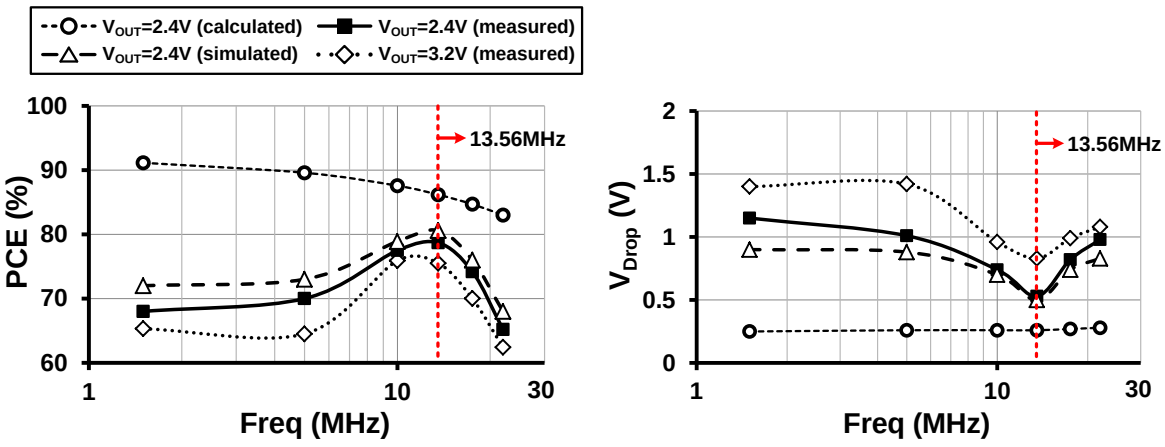
increases above 1 kΩ, I_{Load} drops and P_{Load} for the same V_{OUT} decreased. Therefore, the internal power dissipation ($P_{Tr.sw}$ + P_{CMP}) in (2.5) becomes more dominant, reducing the PCE. On the other hand, when R_L decreased below 1 kΩ, higher input current is required to drive the heavy load, increasing $P_{Tr.Ron}$ and V_{Drop}, as shown in Fig. 2.23b, and resulting in the PCE to decrease.



(a) (b)

Fig. 2.23. Measured (a) PCE and (b) V_{Drop} vs. R_L with V_{OUT} = 2.4 and 3.2 V, C_{IN} = C_L = 1 µF, and f_c = 13.56 MHz.

Fig. 2.24 shows the measured, simulated, and calculated PCE and V_{Drop} vs. f_c with R_L = 1 kΩ. The comparator offsets of the proposed voltage doubler were designed for operation around f_c = 13.56 MHz. The PCE in Fig. 2.24a sharply decreased at higher f_c because the comparator delays became too long and allowed for back current to flow from C_L back to the L_2C_2 tank. At lower operating frequencies the PCE decreased again, though at a slower rate, due to the fixed comparator offsets and CS inverter delays leading the pass transistors to turn off earlier than they should, thus conducting smaller amount of power to the load. Fig. 2.24b shows the measured V_{Drop} vs. f_c, which is also affected by the switching times. Even though V_{OUT} and R_L were fixed in all frequencies, lower PCE required higher input power to achieve the same V_{OUT}. Therefore, V_{Drop} increased at frequencies that had lower PCE.



(a) (b)

Fig. 2.24. Measured (a) PCE and (b) V_{Drop} vs. f_c with V_{OUT} = 2.4 and 3.2 V, R_L = 1 kΩ, and C_{IN} = C_L = 1 μF.

We have measured three different chips, all of which showed similar characteristics as in Fig. 2.22 ~ 2.24, where the measured PCE is slightly lower than the simulated PCE due to process variations. Since the active voltage doubler has been optimized for a certain operating condition, i.e. V_{OUT} = 2.4 V, R_L = 1 kΩ, and f_c = 13.56 MHz, the PCE somewhat deviates from its optimal point when the operating condition changes. However, the voltage doubler still operates properly with PCE > 74% within the range of V_{OUT} (2 ~ 4 V) and R_L (0.5 ~ 1.5 kΩ), as long as f_c remains at 13.56 MHz. f_c is unlikely to change, because it is often controlled externally by a crystal-based oscillator that drives the power amplifier, shown in Fig. 2.1. The best way to oppose such PCE deviations from the optimal point is to form another closed loop around the voltage doubler at the system level to monitor V_{OUT} and change CTL0:3 at any operating condition via a well-defined search algorithm.

Fig. 2.25 shows post-layout simulated power consumption in the key components of the active voltage doubler in a pie-chart, when $V_{IN,peak}$ = 1.45 V, V_{OUT} = 2.4 V, R_L = 1 kΩ, C_{IN} = C_L = 1 μF, and f_c = 13.56 MHz. It can be seen that 80% of the input power has been delivered to the load, while the majority of the remaining 20% dissipates in the pass transistors (N_1 and P_1), followed by the comparators (CMP_N and CMP_P). Losses in N_1 (6.3%) and P_1 (6.4%) are due to their R_{on}, which are represented in our model by $P_{Tr.Ron}$.

Power dissipation in CMP_N (2.6%) and CMP_P (4.6%) include the comparators' internal power consumption as well as the switching loss, which are represented in the model by P_{CMP} and $P_{Tr.sw}$, respectively. In addition, the offset-controlled functions in CMP_N and CMP_P consume only 29 µW and 45 µW, which are 0.4% and 0.6% of the total power consumption, respectively.

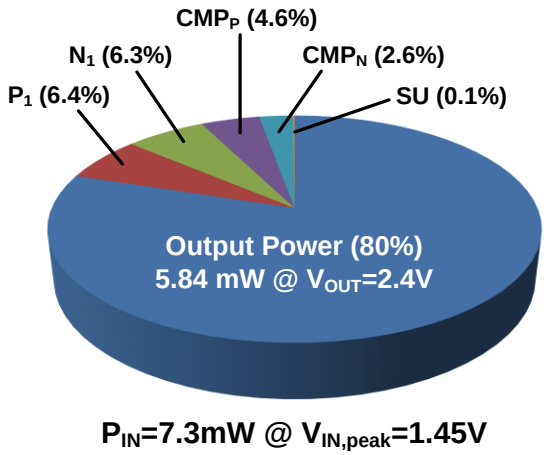


Fig. 2.25. Simulated power consumption pie-chart when $V_{IN,\,peak}$ = 1.45 V, V_{OUT} = 2.4 V, R_L = 1 kΩ, C_{IN} = C_L = 1 µF, and f_c = 13.56 MHz.

Table 2.3 benchmarks several recently reported rectifiers and voltage doublers used in various power-management blocks along with the proposed active voltage doubler. In rectifiers, a major limitation is that V_{OUT} is always less than $V_{IN,Peak}$, as expected. Passive voltage doublers cannot provide high PCE for the reasons discussed in section 2.3.1. Two active voltage doublers have been recently reported in the literature for energy scavenging from mechanical vibrations via piezoelectric transducers, which are designed to operate at low frequencies in the order of 100 Hz [43], [44]. Even though these active voltage doubles offer high PCE, they are not suitable for inductively powered biomedical applications, which operate at much higher frequencies through near-field inductive links.

What we have presented in the last column is, to the best of our knowledge, the first active voltage doubler that can operate at 13.56 MHz in the ISM-band, providing 2.4 V of DC supply to a 1 kΩ load from a peak AC input voltage of only 1.46 V, while

offering the highest measured PCE of 79%. This is made possible with the accurate timing provided by offset-controlled high speed comparators for both rising and falling slopes of the carrier signal to maximize the power delivered to the load when turning the pass transistors on, while minimizing the back currents when turning them off. Table 2.4 summarizes the specifications of the active voltage doubler and the inductive link used in our measurements.

Table 2.3: Rectifier and voltage doubler benchmarking

Publication		2009 [32]	**This work**	[66]	2009 [27]	2011 [28]	2008 [43]	2011 [44]	**This work**
Technology		0.18 µm CMOS	**0.5 µm CMOS**	Discrete (1N4148)	0.18 µm CMOS	0.8 µm HVCMOS	0.35 µm CMOS	Discrete	**0.5 µm CMOS**
Structure		Active rectifier	**Active rectifier**	Passive voltage doubler	V_{Th}-cancelled voltage multiplier	V_{Th}-cancelled voltage doubler	Active voltage doubler	Active voltage doubler	**Active voltage doubler**
$V_{IN,\,peak}$ (V)		1.25	**3.8**	2.3	0.8	11.1	N/A	1.2	**1.46**
V_{OUT} (V)		0.96	**3.12**	2.4	1.8	20	3	2.24	**2.4**
VCE (%)*		76.8	**82.1**	52.2	56.3	90.1	N/A	93.3	**82.2**
R_L (kΩ)		2	**0.5**	1	270	20	400	0.1	**1**
C_{IN} / C_L (µF)		- / 200p	**- / 10**	1 / 1	N/A	- / 1	N/A	- / 100	**1 / 1**
f_c (MHz)		10	**13.56**	13.56	13.56	13.56	200 Hz	20 Hz	**13.56**
Area (mm^2)		0.86	**0.18**	N/A	0.83	N/A	N/A	N/A	**0.144**
PCE (%)	Sim.	N/A	**87**	N/A	N/A	90.5	95	N/A	**80**
	Meas.	76	**80.2**	51	54.9	N/A	> 90	83	**79**

* Voltage conversion efficiency (VCE) = V_{OUT} / ($V_{IN,peak}$ × multiplication factor)

** On-chip capacitor. All other C_{IN} and C_L are off-chip components.

Table 2.4: Additional active voltage doubler specification

$V_{Th(N)}$ / $V_{Th(P)}$	0.75 V / 0.9 V
Nominal output power	4 ~ 20 mW
Input capacitor (C_{IN}) / Load capacitor (C_L)	1 µF / 1 µF
Output ripple (R_L = 1 kΩ)	22 mV_{pp}
Comparator power consumption	0.1 ~ 0.8 mW*
Primary coil diameter / Inductance (L_1)	16.8 cm / 0.88 µH
Secondary coil diameter / Inductance (L_2)	3.0 cm / 0.41 µH
Pass transistor P_1 size (W_p / L_p)	2100 µm / 0.6 µm
Pass transistor N_1 size (W_n / L_n)	1200 µm / 0.6 µm
Total area on chip	0.144 mm^2

*From simulation

CHAPTER III

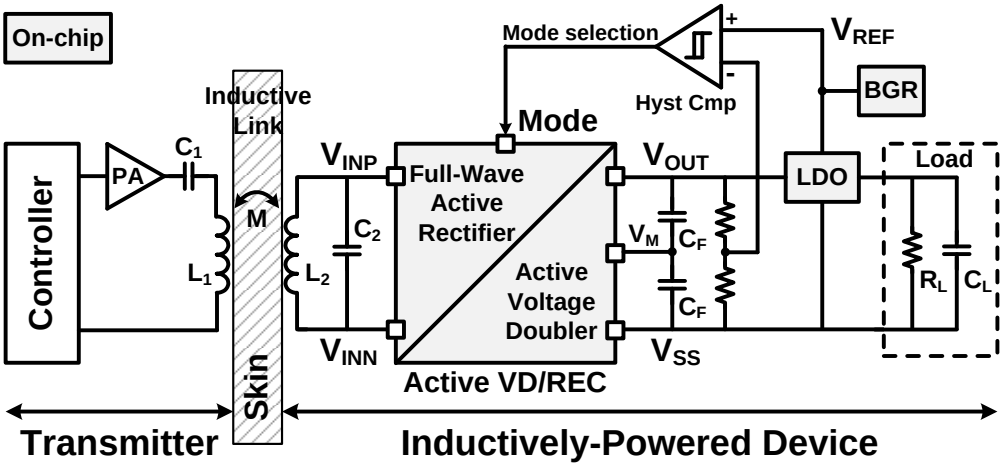
AN ADAPTIVE RECONFIGURABLE VOLTAGE DOUBLER/RECTIFIER (VD/REC) FOR EXTENDED-RANGE INDUCTIVE POWER TRANSMISSION

3.1. Introduction

Active rectifiers and voltage doublers using synchronous switches have been widely used to convert AC input signals to DC outputs for inductively powered applications [18]-[44]. Rectifiers require higher peak inputs than the desired outputs, which may be temporarily limited by the weak coupling of the inductive links. On the contrary, active voltage doublers are capable of generating higher output voltages, but their power conversion efficiencies (PCE) are generally lower than active rectifiers with similar size. In order to address such limitations, we have proposed a power-efficient reconfigurable active voltage doubler/rectifier (VD/REC) for robust wireless power transmission through inductive links over an extended range. Both voltage doubler (VD) and rectifier (REC) modes are integrated into a single structure, employing low dropout active synchronous switches, leading to high PCE. Moreover, by adding an output voltage sensing circuit, VD/REC can automatically change its operating mode to either VD or REC depending on which one is a better choice for generating the desired output voltage to accommodate with a wider range of mutual coil arrangements.

Fig. 3.1 shows the block diagram of a wireless power transmission link that includes the proposed VD/REC. A power amplifier (PA) drives the primary coil, L_1, at the designated carrier frequency, (f_c = 13.56 MHz), which improves the coils' quality factors (Q) and increases the overall power transmission efficiency, while maintaining the sizes of LC components small for implantable applications [17]. Coupled signal across the secondary, L_2, creates an AC voltage, V_{IN} (= V_{INP} - V_{INN}), across L_2C_2 which is tuned at f_c. VD/REC, which follows the L_2C_2 tank, converts V_{IN} to an automatically adjusted DC voltage, V_{OUT}, for supplying the load after regulation. If V_{IN} falls below a certain

level, which is determined by comparing a portion of V_{OUT} with a reference voltage, V_{REF}, using a hysteresis comparator, then Mode = 1 and VD/REC operates in VD mode. Since the voltage doubler can generate the desired V_{OUT} with much lower V_{IN} than the rectifier, VD/REC can still provide sufficient V_{OUT} to the load even with decreased V_{IN}. On the other hand, if V_{IN} increases above V_{REF} + hysteresis window, then Mode = 0 and VD/REC will operate in the REC mode, which can achieve higher PCE than the VD mode while generating the desired V_{OUT}.



Condition	Mode	Operation	Key Feature
$V_{OUT} > V_{REF(Hyst)}$	0	Full-wave rectifier	High power efficiency (PCE)
$V_{OUT} < V_{REF(Hyst)}$	1	Voltage doubler	High output voltage (V_{OUT})

Fig. 3.1. Block diagram of an inductively powered device with emphasis on the wireless power transmission through the proposed active VD/REC converter.

3.2. Active VD/REC Architecture

3.2.1. Concept of the Active VD/REC

The concept of active VD/REC starts from combining two separate AC-to-DC converters, a rectifier and a voltage doubler, into a single structure in which the operating mode, REC or VD, is selected by an external mode selection signal. Fig. 3.2 shows the conceptual diagram of the active VD/REC converter which consists of the full-wave rectifier and the voltage doubler with active diodes. The full-wave rectifier requires two

diodes, D_1 and D_2, and a cross-coupled NMOS pair, N_1 and N_2. Either D_1-N_2 path or D_2-N_1 path is activated depending on the amplitude of V_{INP} and V_{INN} to transfer the input power to the output filtering capacitors, $C_F/2$. The voltage doubler requires only two diodes, D_1 and D_{N1}, charging one C_F per half cycle depending on the polarity and amplitude of V_{IN} (= V_{INP} - V_{INN}). Therefore, V_{OUT} becomes almost doubled compared to the peak voltage of V_{IN}. In order for VD/REC to include both structures, D_1 is shared, and D_2 and N_2 have enable functions to turn them on/off in the REC and VD modes, respectively. N_1 operates as part of a cross-coupled pair in the REC mode, while it is reconfigured as an NMOS diode, D_{N1}, in the VD mode. V_{INN} and V_M are also shorted through a switch, N_3, in the VD mode. VD/REC utilizes active diodes, D_1, D_2, and D_{N1}, in which rectifying pass transistors are driven by fast comparators to operate as switches in the deep triode region with low dropout voltages. Therefore, these active diodes dissipate less power compared to passive diodes, leading to higher PCE in both operating modes.

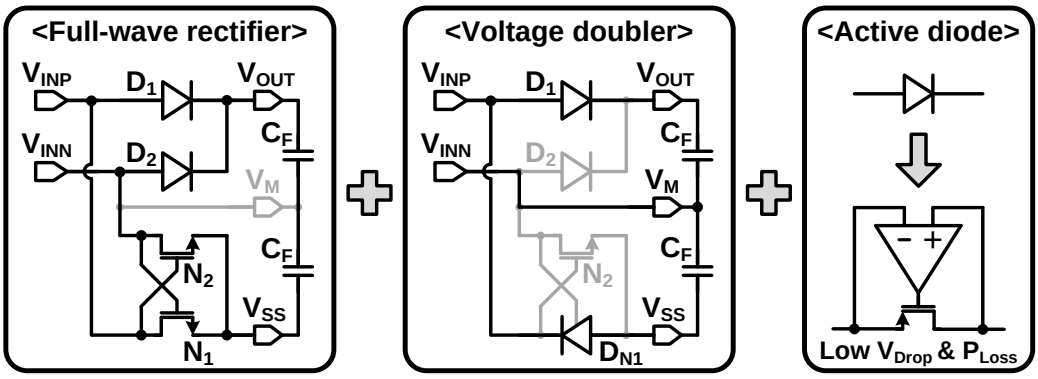


Fig. 3.2. Conceptual diagram of the active VD/REC converter in which a full-wave rectifier and a voltage doubler are combined using active diodes.

3.2.2. Implementation of the Active VD/REC

Fig. 3.3 shows a simplified schematic diagram of the VD/REC, consisting of PMOS and NMOS active diodes, D_1, D_2, and D_{N1}, in which pass transistors, P_1, P_2, and N_1, are driven by high- speed comparators, CMP_{P1}, CMP_{P2}, and CMP_{N1}, respectively, to

minimize AC-DC dropout voltage and power loss. Mode signals, EN and EN_B, which are derived from the mode control circuit, can reconfigure the VD/REC topology for rectification or doubling functions, as shown in Fig. 3.2. In the REC mode (EN, EN_B = 0, 1), gates of N_1 and N_2 are connected to V_{INN} and V_{INP}, respectively, resulting in a cross-coupled NMOS pair with positive feedback, while CMP_{N1} is deactivated. Both PMOS active diodes are utilized in this mode, alternating every half cycle to transfer input power to the load. For example, when $V_{INP} > V_{INN}$, N_2 turns on while N_1 turns off. Then, when $V_{INP} > V_{OUT}$, CMP_{P1} output goes low turning P_1 on with a low dropout voltage. The input current in this case flows from V_{INP} through P_1 to charge $C_F/2$ and returns back to V_{INN} through N_2. In the VD mode (EN, EN_B = 1, 0), P_2 and N_2 are always off and CMP_{P2} is deactivated. Only P_1 and N_1 operate as active diodes, while N_3 strongly connects V_{INN} to V_M for charging the filtering capacitors, C_F, one per half cycle, to almost double V_{OUT} in reference to V_{SS}.

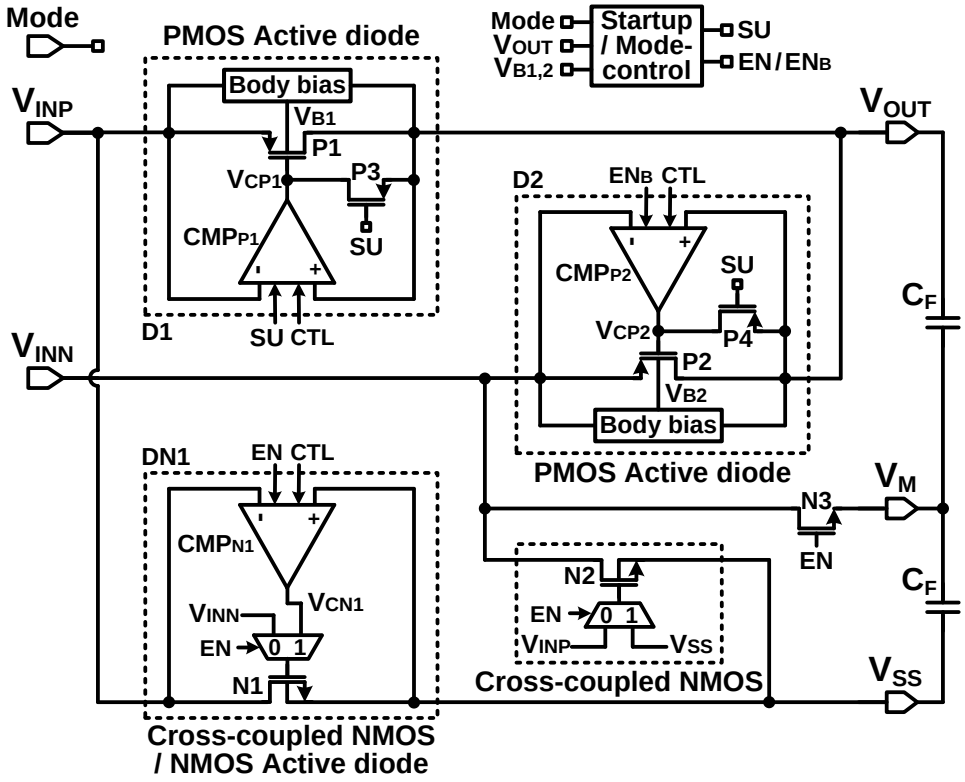


Fig. 3.3. Schematic diagram of the proposed VD/REC employing active diodes to achieve lower dropout voltage and higher PCE for both REC and VD modes.

Since the comparators in active diodes are supplied from V_{OUT}, which is initially at 0 V, self-startup capability is a feature necessary in active VD/REC. The startup circuit in Fig. 3.3 monitors V_{OUT} and sets SU = EN = EN_B = 0 when V_{OUT} is too low. At startup, N_1 and N_2 are cross-coupled through MUXs, and P_1 and P_2 are diode-connected through P_3 and P_4, respectively, forming a passive rectifier, which charges V_{OUT} regardless of the comparators' status up to the point where V_{OUT} reaches a desired level. Then SU toggles to enable VD/REC to operate normally. PMOS body terminals, V_{B1} and V_{B2}, are always connected to the highest potential among $V_{INP,N}$ and V_{OUT} via their body bias circuits.

3.3. Circuit Details and Design Considerations

In order to drive large pass transistors at 13.56 MHz, comparators need to have short turn-on/off delays, which may otherwise reduce the PCE by either decreasing the input power delivered to the load or allowing instantaneous reverse current back from C_F. We have used high speed comparators with built-in triple offset-control functions to expedite V_{OUT} transitions by compensating for both turn-on/off delays, which was introduced in section 2.3.

Fig. 3.4 shows the schematic diagram of the high speed comparator, CMP_P, which is equipped with three offset-control functions: turn-on, turn- off, and output locking offsets. In Fig. 3.4, P_6, P_7, N_7, N_8, P_{11}, and N_{14} form a common-gate comparator, in which input voltages (V_{OUT}, $V_{INP,N}$) are applied to the sources of P_6 and P_7. Turn-on offset block, consisting of P_8-P_9 current sources and P_{10} control switch, injects additional offset current to force V_1 to increase earlier, leading to fast turn-on of $P_{1,2}$ in Fig. 3.3. The offset control signal, V_{OS1P}, deactivates P_{10} just after turning $P_{1,2}$ on and activates it again after the current-starved inverter (INV_1 and N_{15}) delay, which does not need to be accurate as long as it is shorter than one carrier cycle. Turn-off offset function utilizes the size mismatch between N_7 and N_8, where the larger N_8 pulls additional current from V_1 node, forcing V_1 to start dropping earlier to turn $P_{1,2}$ off at the right time. After the comparator output, V_{CP},

goes high and turns $P_{1,2}$ off, N_{11} is activated by V_{OS2P} for the current-starved inverter delay time to keep V_1 low and prevent V_{CP} from bouncing due to $V_{INP,N}$ variations. CMP_N has a similar but symmetrical structure. In addition, 4-bit off-chip digital control signals, CTL0:1 for CMP_P and CTL2:3 for CMP_N, are utilized to adjust the switching times of VD/REC against process variations.

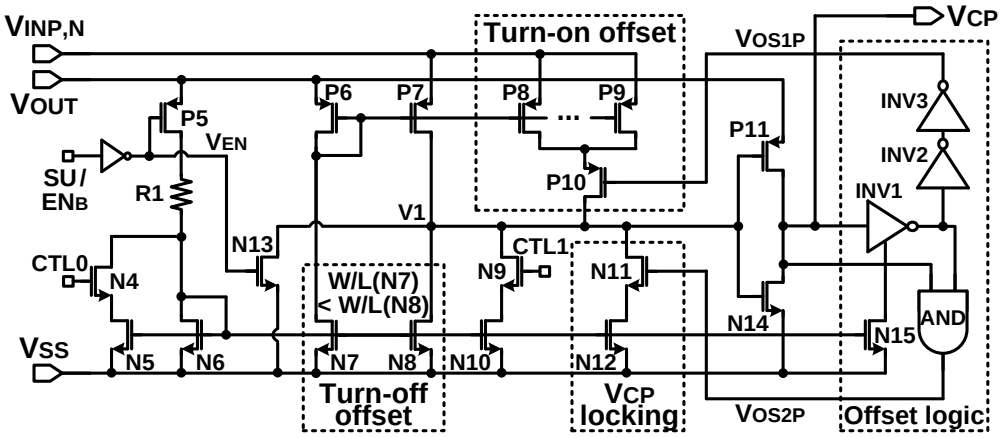


Fig. 3.4. Schematic diagram showing three built-in triple offset-control functions, which are turn-on, turn-off, and output locking offsets, in our high speed comparator, CMP_P.

In the startup circuit in Fig. 3.5a, when V_{OUT} is very low, P_{12} turns off and SU goes low, resulting in P_1 and P_2 in Fig. 3.3 to stay diode-connected through P_3 and P_4, respectively. During the same period, both EN and EN_B of the mode control circuit in Fig. 3.5b become low, so all comparators are in the sleep mode while N_1 and N_2 are cross-coupled through MUXs, leading the VD/REC to operate as a passive rectifier. With SU = EN_B = 0, N_{13} in Fig. 3.4 forces $V_{CP1,2}$ to be high, further supporting P_1 and P_2 to be diode-connected. When $V_{OUT} > V_{Th(N16)} + V_{Th(P12)}$, SU toggles high, turning P_3 and P_4 off, releasing the comparator outputs, and allowing P_1 and P_2 to operate as switches. The mode control circuit consists of two pairs of level-shifters and logic gates, one of which is shown in Fig. 3.5b, to level-shift the Mode signal to either V_{B1} or V_{B2} (in Fig. 3.3) for creating EN and EN_B signals, which control various switches at proper voltage levels. In Fig. 3.5c, the body bias circuit automatically connects V_{B1} and V_{B2} to max(V_{INP}, V_{OUT}) and max(V_{INN}, V_{OUT}), respectively, through P_{17} and P_{18} [18].

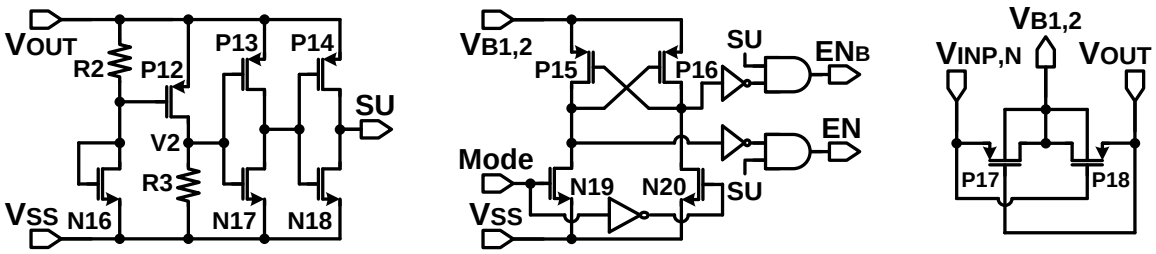


Fig. 3.5. Schematic diagrams of the (a) startup circuit, (b) mode control circuit, and (c) body bias circuit.

3.4. Measurement Results

VD/REC was fabricated in the ON-Semiconductor 0.5-μm 3M2P n-well standard CMOS process, occupying 0.585 mm^2. Fig. 3.6 shows the chip micrograph and floor plan of the VD/REC, low-dropout regulator (LDO), and bandgap reference (BGR). The sizes of the main rectifying transistors are as follow: $W_{P1,2}$ = 3300 μm, $W_{N1,2}$ = 1800 μm, and W_{N3} = 12000 μm with the minimum length of L = 0.6 μm.

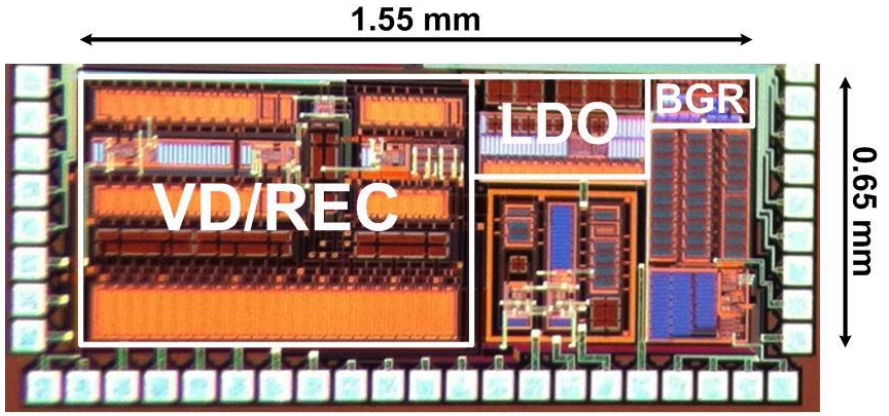


Fig. 3.6. Fabricated chip micrograph of the VD/REC in ON-Semiconductor 0.5-μm standard CMOS process, occupying an area of 0.585 mm^2.

3.4.1. Reconfigurable VD/REC Waveforms

Fig. 3.7 shows measured input/output waveforms in the REC and VD modes with $R_L \parallel C_F/2$ = 1 kΩ || 0.5 μF (no regulator) at f_c = 13.56 MHz. The same supply voltage was applied to the PA on the primary side to verify the V_{OUT} difference between the REC and VD modes. In the REC mode (Mode = 0), V_{INP} and V_{INN} charge V_{OUT} alternatively,

resulting in $V_{IN,peak(REC)}$ = 3.35 V and V_{OUT} = 2.7 V. In the VD mode (Mode = 1), V_{INN} is shorted via N_3 to V_M, the middle voltage of V_{OUT}, and V_{INP} goes well above $V_{IN,peak(REC)}$ to achieve V_{OUT} = 3.55 V with $V_{IN,peak(VD)}$ = 2.6 V. Large instantaneous input currents flow into the VD/REC during the conduction period, inducing the voltage drop across N_3, which is V_{INN} - V_M. $V_{IN,peak(VD)}$ is less than $V_{IN,peak(REC)}$ because of a reduction in the inductive link Q-factor due to higher input and output currents in the VD mode.

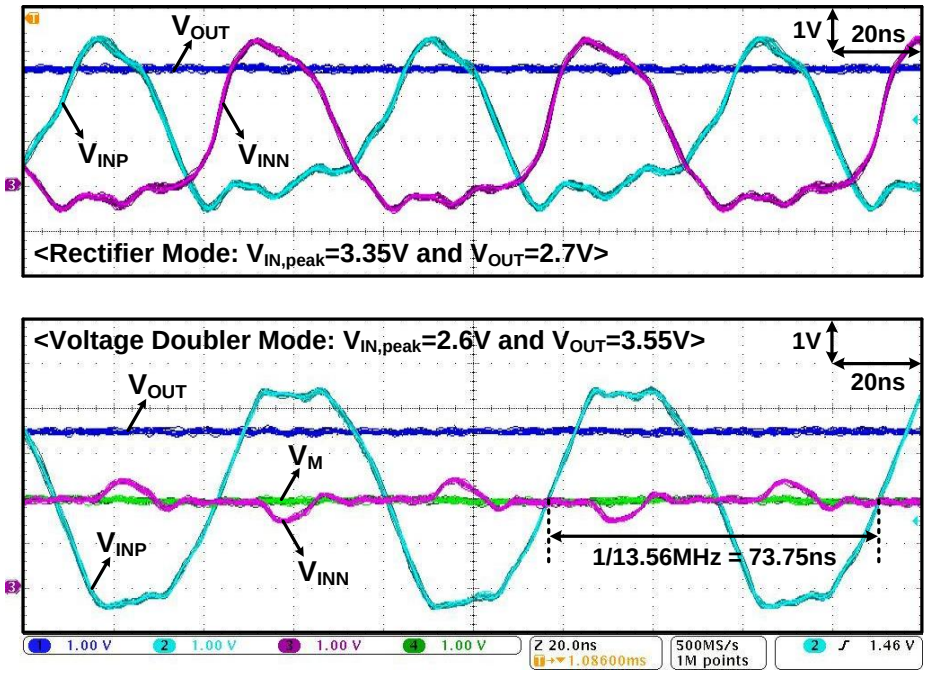


Fig. 3.7. Measured input/output voltage waveforms in the REC (top) and VD (bottom) modes when R_L || $C_F/2$ = 1 kΩ || 0.5 µF (no regulator) and f_c = 13.56 MHz.

3.4.2. Power Transmission Range and PCE Measurements

In order to verify the benefits of using the VD/REC over a rectifier, we have measured $V_{IN,peak}$ and V_{OUT} while sweeping the relative distance (d) and orientation (θ) between a pair of coupled coils, L_1 and L_2, as shown in Fig. 3.8. In this test setup, which specifications are shown in Table 3.2, a class-C power amplifier on the transmitter side (Tx) drives the inductive link to induce a 13.56 MHz sinusoidal signal across the VD/REC.

Fig. 3.9 shows the measured $V_{IN,peak}$ and V_{OUT} vs. d and θ, and demonstrates how using the VD/REC extends the inductive link power transmission range in terms of the coils' relative distance and angular misalignment compared to REC-only. Hysteresis window of the off-chip comparator was set to 2.6 ~ 3.7 V, and indicated on the graphs as horizontal dashed lines. In the d-sweep test, the VD/REC operates in the REC mode when d is small. V_{OUT} drops as d increases, and when d > 5.5 cm, VD/REC switches to the VD mode, increasing V_{OUT} by 0.8 V (30.8%). As a result, VD/REC maintains sufficient V_{OUT} > 2.5 V for coil separations up to d = 8 cm, compared to the REC-only, which fails at d > 6 cm (a 33% improvement). Similarly, VD/REC improved the inductive link tolerance to coil rotations by extending the range from θ = 53° (REC-only) to 75° (VD/REC) at d = 3 cm (a 41.5% improvement).

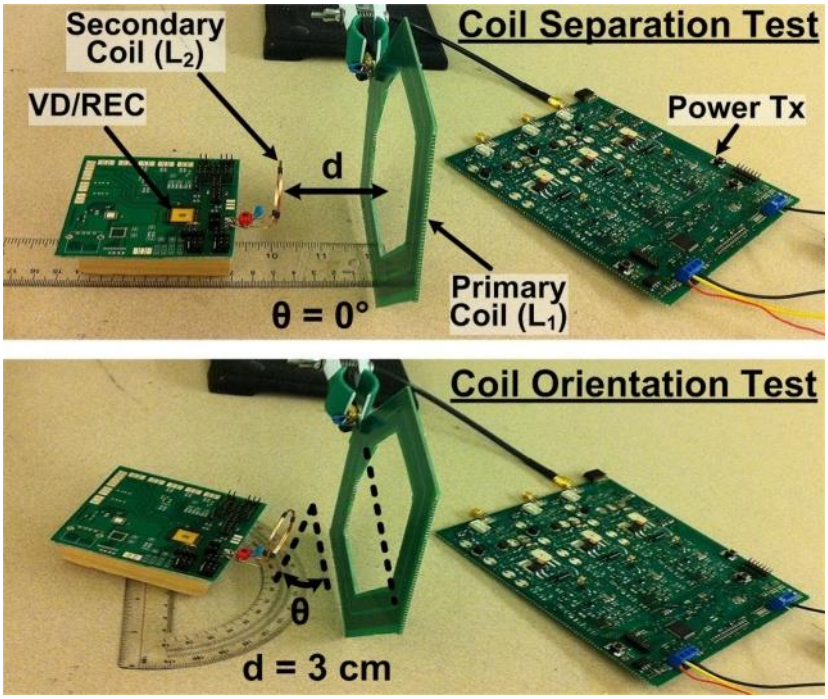


Fig. 3.8. Test setup for measuring the PCE and input/output voltages of the active VD/REC AC-to-DC converter when sweeping the relative coil distance (top) and orientation (bottom).

To consider the practical conditions in which the output voltage of the VD/REC varies due to coil misalignments as well as loading changes, we measured the PCE while sweeping V_{OUT} by adjusting the Tx output power delivered to the primary coil, L_1. The

PCE of VD/REC can be defined as the delivered power to the load over the input power from the L_2C_2 tank. Fig. 3.10 shows the measured PCE vs. V_{OUT} in both REC and VD modes with R_L = 0.5 kΩ and 1 kΩ at f_c = 13.56 MHz. The highest PCEs of the REC and VD modes were 77% and 70%, respectively, at V_{OUT} = 3.1 V with R_L = 0.5 kΩ. PCE drop for V_{OUT} > 3.7 V and V_{OUT} < 2.8 V are mainly due to the pass transistor sizing and comparator offsets which were designed for V_{OUT} = 2.8 ~ 3.7 V. The VD/REC still operates properly against V_{OUT} variations with PCE > 74% within V_{OUT} = 2.6 ~ 4.3 V in the REC mode and PCE > 68.5% within V_{OUT} = 2.5 ~ 3.7 V in the VD mode for R_L = 0.5 kΩ. The V_{OUT} range is determined based on the hysteresis comparator window of 2.6 ~ 3.7 V. Table 3.1 benchmarks the proposed active VD/REC against several recently reported rectifiers and voltage doublers. Table 3.2 provides a few additional specifications of the VD/REC and the inductive link used in our measurements.

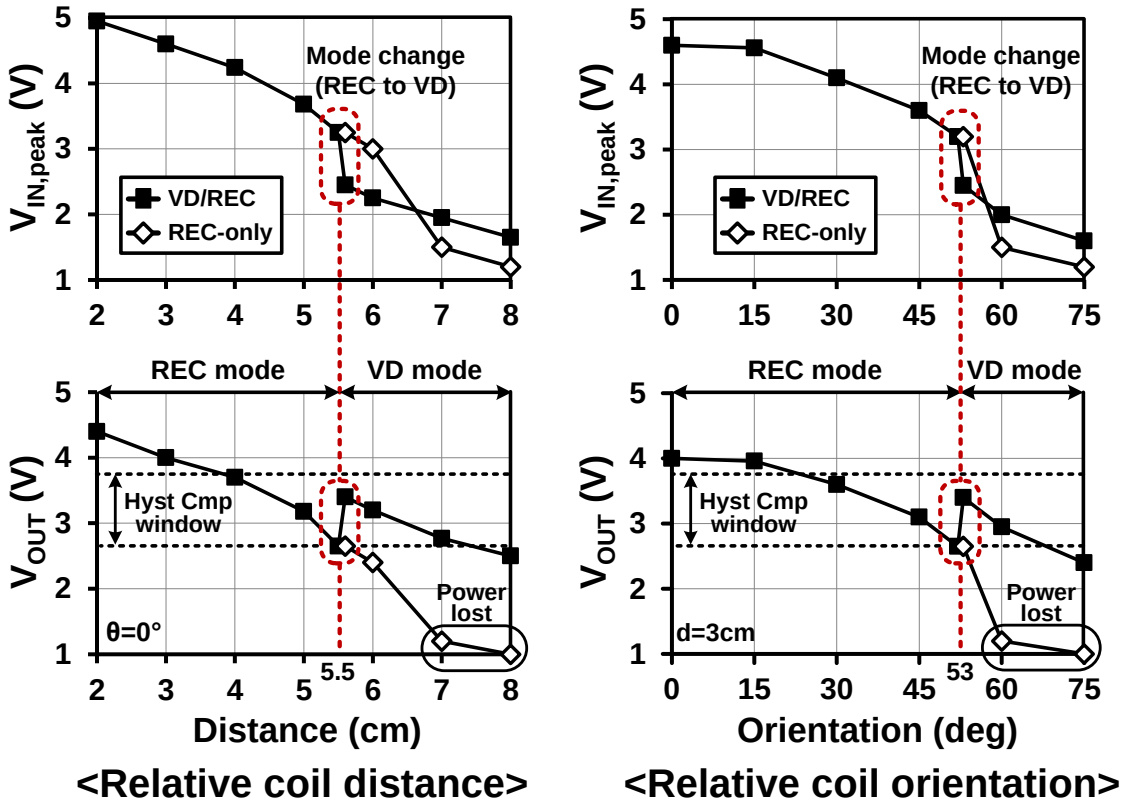


Fig. 3.9. Measured input and output voltages while sweeping the coils relative distance (d) and orientation (θ) in Fig. 3.8, which clarify that using VD/REC extends the inductive link power transmission range.

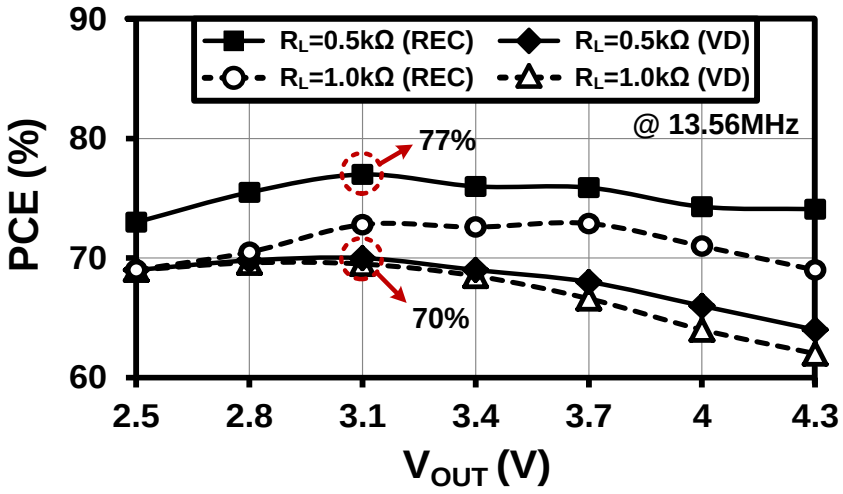


Fig. 3.10. Measured PCE vs. V_{OUT} with R_L = 0.5 kΩ and 1 kΩ at f_c = 13.56 MHz, leading to the highest PCEs of 77% and 70% in the REC and VD modes, respectively.

Table 3.1: Rectifier and voltage doubler benchmarking

Publication		2009 [32]	2012 [67]	2010 [27]	2011 [28]	**This work**	
Technology		0.18µm	0.18µm	0.18µm	0.8µm	**0.5µm CMOS**	
Structure		REC	REC	Multiplier	VD	**Active VD/REC**	
						VD	**REC**
$V_{IN,\,peak}$ (V)		1.25	1.5	0.8	11.1	**2.15**	**3.7**
V_{OUT} (V)		0.96	1.33	1.8	20	**3.1**	**3.1**
VCE (%)*		76.8	89	56.3	90.1	**72.1**	**83.8**
R_L (kΩ)		2	1	270	20	**0.5**	
f_c (MHz)		10	13.56	13.56	13.56	**13.56**	
Area (mm^2)		0.86	0.009	0.83	N/A	**0.585**	
PCE (%)	Sim.	N/A	N/A	N/A	90.5	**75**	**81**
	Meas.	76	81.9	54.9	N/A	**70**	**77**

* Voltage conversion efficiency (VCE) = V_{OUT} / ($V_{IN,peak}$ × multiplication factor)

Table 3.2: Additional active VD/REC specifications

Nominal output power	6 ~ 37 mW
Output filtering capacitor (C_F)	1 µF
Output ripple (R_L = 0.5 kΩ)	50 mV_{pp}
Bandgap reference voltage (V_{REF})	1.187 V
Primary coil diameter / inductance (L_1)	16.8 cm / 0.88 µH
Secondary coil diameter / inductance (L_2)	3.0 cm / 0.41 µH
Total area of the VD/REC	0.585 mm^2

3.4.3. *In Vitro* Experiments

Inductively powered IMDs that employ the active VD/REC converter need to be hermetically sealed in biocompatible materials and placed in the conductive tissues environment with high permittivity, which can affect not only the secondary coil characteristics but also the VD/REC performance [68]. In order to emulate the implant environment, we conducted *in vitro* experiments with the test setup in Fig. 3.11, in which the secondary coil (L_2) was wrapped in a piece of steak (bovine sirloin).

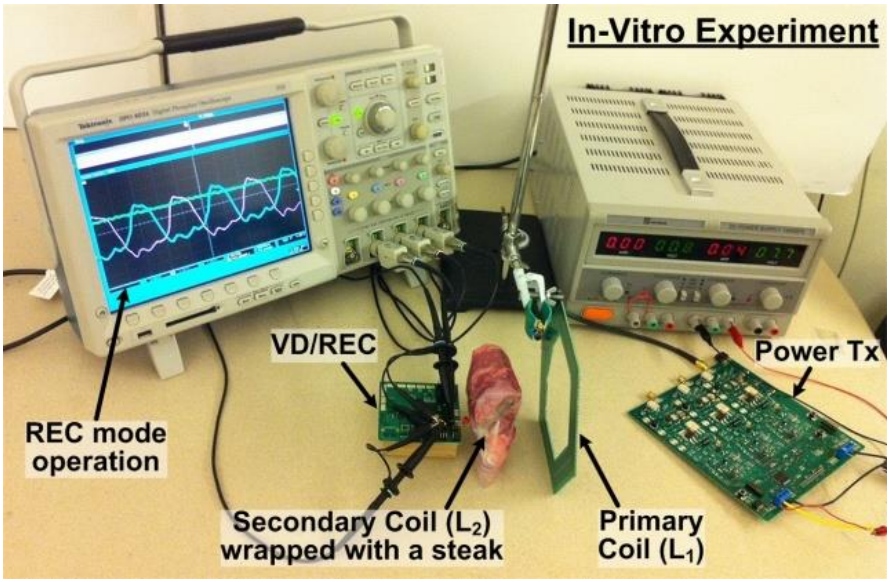


Fig. 3.11. Test setup for *in vitro* experiments that resemble an IMD environment with the secondary coil, L_2, wrapped in a piece of steak.

Fig. 3.12 shows the measured $V_{IN,peak}$ and V_{OUT} while sweeping the coils' relative distance (d) in the air (Fig. 3.8) and muscle (Fig. 3.11) environments. The muscle environment leads to a small reduction in both $V_{IN,peak}$ and V_{OUT} compared to the air environment when d is increased. This is because wrapping L_2 with a piece of steak increases its parasitic capacitance and resistance, leading the quality factor (Q) of the secondary coil to decrease and the power loss in its parasitic resistance to increase. However, these curves show that using the VD/REC still extends the inductive link power transmission range in both environments to $d > 8$ cm.

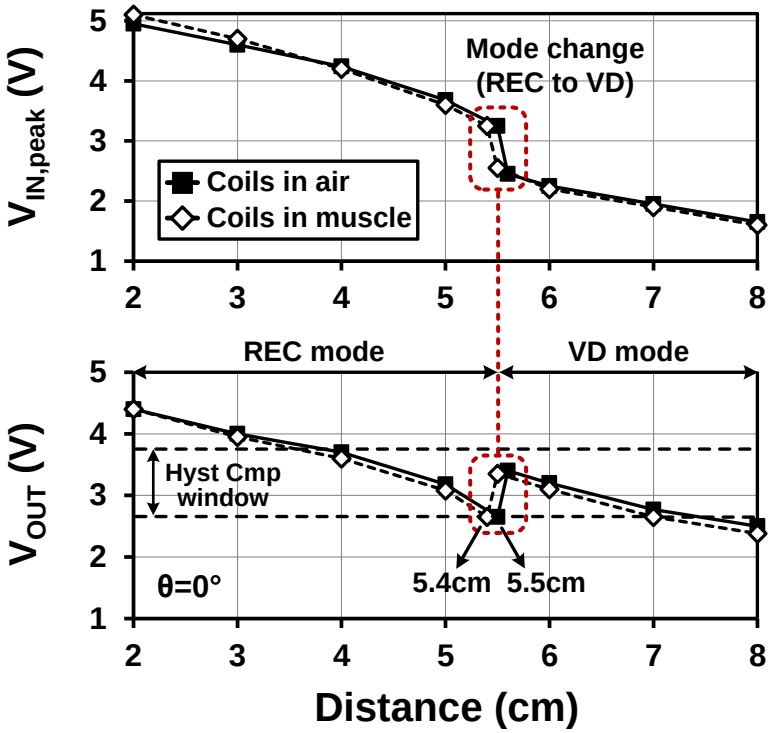


Fig. 3.12. Measured input and output voltages while sweeping the coils' relative distance in the air (Fig. 3.8) and muscle (Fig. 3.11) environments.

CHAPTER IV

POWER-MANAGEMENT CIRCUITS FOR WIRELESS BIOMEDICAL MICROSYSTEMS

The proposed active AC-to-DC converters in chapter 2 have been adopted in several wireless biomedical microsystems developed in GT-bionics lab, such as a wireless integrated neural-recording system (WINeR) in [65] and an intraoral tongue-drive system (iTDS) in [69], to provide sufficient wireless power through the inductive link while achieving high power conversion efficiency (PCE). Moreover, these biomedical systems have been equipped with additional power-management and data telemetry functions: 1) low-dropout regulators (LDO) to generate constant supply voltages, 2) forward and back data telemetry for bi-directional communication through the inductive link, 3) an overvoltage protection circuit for safe inductive power transmission, and 4) battery charging and monitoring circuits to provide an alternate energy source when the inductive power is interrupted or insufficient.

4.1. Wireless Integrated Neural-recording System (WINeR)

4.1.1. Power-management Circuits in WINeR

Our GT-bionics lab presented an inductively powered 32-channel wireless integrated neural recording (WINeR) system-on-a-chip (SoC) in [65], which can be ultimately used for one or more small freely behaving animals in neuroscience applications. In this system, the inductive powering is intended to relieve the animals from carrying bulky primary batteries used in other wireless systems, while enabling long recording sessions. In addition, a proposed on-chip high-efficiency active rectifier with optimized coils help improve the overall system power efficiency, which is controlled in a closed loop to supply stable power to the WINeR regardless of the coil displacements [70]. The proposed power-management circuits in the WINeR system also utilized the

overvoltage protection circuit to control the inductive power level and the load-shift-keying (LSK) back telemetry for reverse data communication.

Key components that are responsible for inductively powering the WINeR system are similar to those used in radio-frequency identification (RFID) systems: power transmitter (Tx), inductive link, and the transponding portion of the WINeR SoC, as shown in Fig. 4.1. On the power Tx side, which can also be referred to the reader or interrogator, a power amplifier (PA) drives the primary coil (L_1) at the power carrier frequency of f_c = 13.56 MHz. We chose this frequency, which is closer to the higher end of the acceptable range for implantable microelectronic devices (IMD), 1~20 MHz, to enhance the quality factor of the coils, which improve the power transfer efficiency (PTE). Another reason was to take advantage of the commercial off-the-shelf (COTS) devices that are available for RFID applications for building the reader.

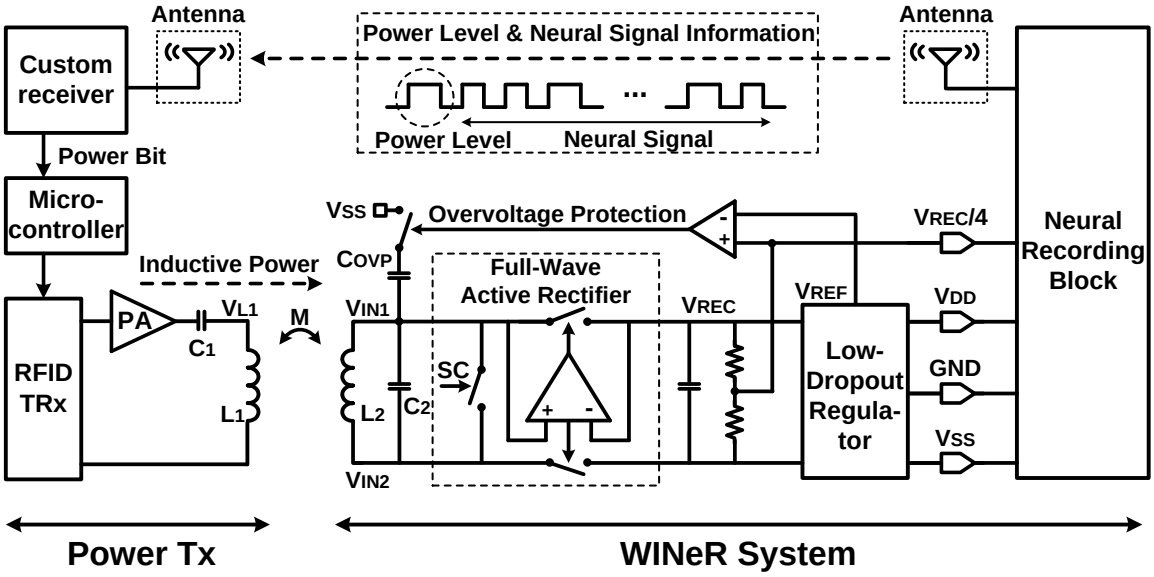


Fig. 4.1. Power-management circuits in the WINeR system.

The power carrier is induced on to the secondary coil (L_2), and generates an AC voltage across the transponder resonance circuit (L_2 and C_2). Following the L_2C_2 tank, there is a full-wave rectifier and a low-dropout regulator to generate V_{REC} and supply lines, respectively, for the rest of the WINeR SoC. The performance of the rectifier is key

to the overall power efficiency of this system because all the usable received power for the WINeR SoC has to pass through this block. Achieving a high PCE is generally important in inductively powered IMDs because it allows them to operate with smaller induced power from a longer distance, lowering the heat dissipation on both sides of the inductive link, which can cause tissue damage if it results in temperature rise beyond safe limits [71]. We utilized a full-wave active rectifier proposed in chapter 2, which is equipped with offset-controlled high speed comparators that provide high PCE at high frequency (13.56 MHz). Thanks to the offset-control functions that compensate for both turn-on and turn-off delays in operating the main rectifying switches, the rectifier conducts for the maximum possible period of time and delivers maximum forward current to the load, while minimizing the back current. Moreover, the closed-loop power control function detects the rectifier output voltage and sends the power level information through antennas, while the power Tx adaptively controls the PA supply voltage to maintain the WINeR supply voltage constant despite the coils' coupling variations [70].

In addition, the rectifier block has a built-in LSK back telemetry mechanism, using short-coil (SC) switches explained in Fig. 2.2, that is utilized to inform the reader about the status of the IMD, deliver measured bio-signals, or close the power control loop [65], [70]. When the data signal is high, the input nodes of the rectifier are shorted together, leading to increased secondary quality factor, Q_2, and increased voltage across the primary coil, L_1. Back telemetry data from the transponder to the reader is detected by sensing these variations across the external LSK sensing block.

The input voltage of the rectifier, $V_{IN} = V_{IN1} - V_{IN2}$, highly depends on the coils mutual coupling, M, which is in turn highly dependent on the coils separation, d, and alignment. Loading variations also change Q_2 and affect V_{IN} even when M is constant. Unexpected variations in M and system power consumption may cause V_{REC} to exceed the safe voltage limits of the application or fabrication process and result in transistor breakdown. To prevent this problem, we have added an overvoltage protection (OVP)

circuit to the rectifier by comparing a quarter of V_{REC} with a constant reference voltage. When V_{IN} exceeds a certain level, the comparator output goes high and a detuning capacitor (C_{OVP}) is added in parallel across the secondary tank circuit, as shown in Fig. 4.1, to reduce V_{IN} by detuning it. The advantage of this method over voltage clamping methods is that no extra heat is dissipated within the ASIC and IMD as a result of this protective safety measure.

4.1.2. Measurement Results

The WINeR SoC was fabricated in the ON Semiconductor 0.5-µm 3-metal 2-poly standard CMOS process. Fig. 4.2 shows the micrograph and floor plan of the chip, which occupies 4.9 x 3.3 mm^2 of silicon area, with emphasis on the power-management circuits.

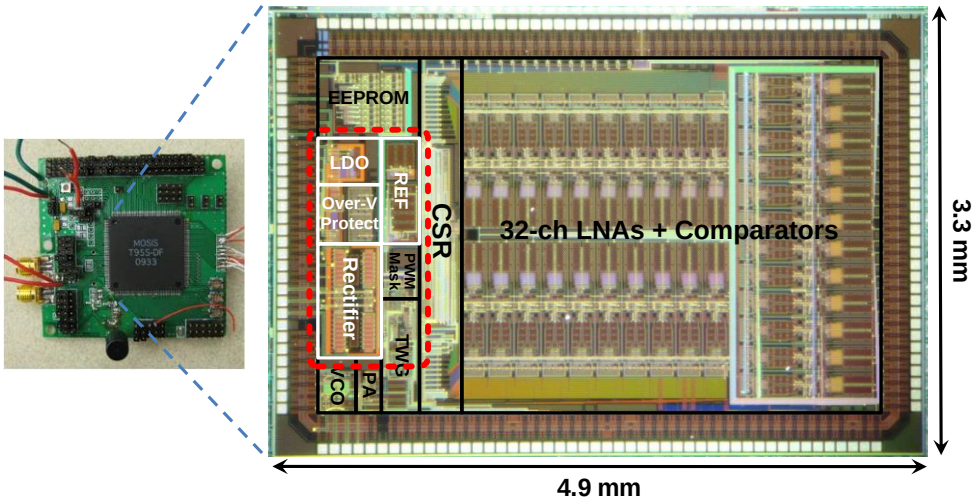


Fig. 4.2. Chip micrograph of the 32-ch WINeR SoC with emphasis on the power-management circuits.

With 3.55 V peak input voltage at 13.56 MHz, the full-wave active rectifier generated 3.12 V output voltage while achieving 80% PCE at 500 Ω load. The nominal distance between primary and secondary coils was 7 cm. Then, the LDO provided the constant supply voltage of 3 V to the rest of the WINeR system. When the closed-loop power control was utilized, the power Tx adaptively controls the transferred power level to maintain the rectifier output voltage to around 3.2 V. Therefore, the LDO output,

which is the system supply voltage, can be constant at 3 V against coil alignments and distance variations. Overall WINeR system specifications can be also found in [65].

To demonstrate the built-in back telemetry capability of our active rectifier, we applied a random stream of serial data bits at 500 kbps and 0.2 µs pulse width (10% duty cycle) to the rectifier short-coil (SC) input terminal in Fig. 4.1. The LSK back telemetry data was recovered using a commercial RFID reader ASIC (TRF7960) from Texas Instruments (Dallas, TX). In Fig. 4.3, measured waveforms from top show the data signal applied to SC, voltages across the load (R_LC_L = 500 Ω || 10 µF), secondary coil (V_{IN1}), primary coil (V_{L1}), and recovered serial data bit stream at TRF7960 output, which has ~1.2 µs delay with respect to SC. Shorting L_2 with SC = High in Fig. 4.1 results in a sudden drop in V_{IN1} and increased current in L_1, which also increases the voltage across L_1. Current and voltage variations in L_1 are detected by the RFID reader and amplitude-shift-keying (ASK) demodulated to recover the LSK back telemetry data. It can be seen in Fig. 4.3 that V_{REC} remains constant during the LSK operation because of the large C_L (10 µF) and small SC duty cycle (10%).

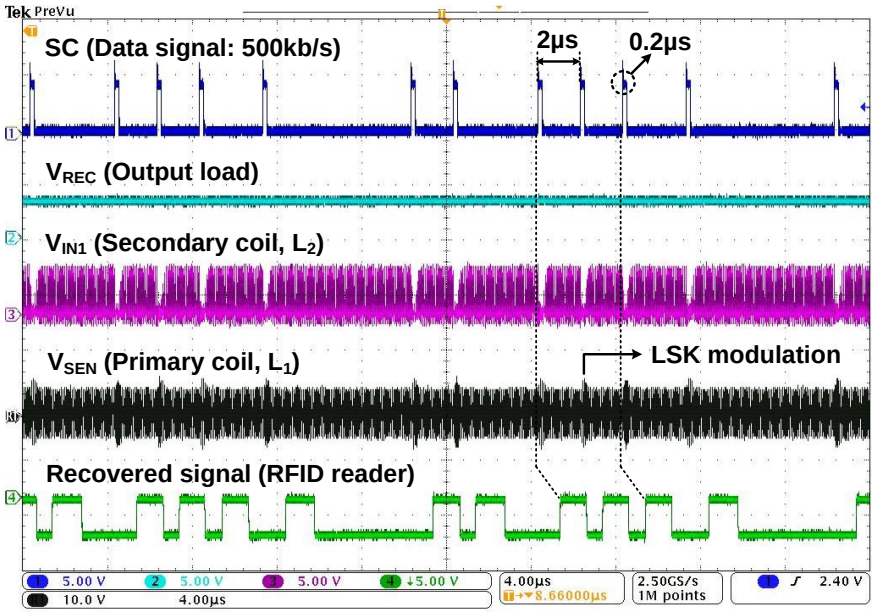


Fig. 4.3. Measured waveforms showing the active rectifier's built-in LSK back telemetry capability through its short-coil (SC) input terminal (data signal = 500 kbps with 10% duty cycle, R_L = 500 Ω, and C_L = 10 µF).

The OVP circuit is activated when V_{REC} increases above a certain threshold voltage, $V_{threshold}$ = 4.4 V, which is determined by comparing $V_{REC}/4$ with a reference voltage, V_{REF} = 1.1 V, generated by the regulator. The comparator in Fig. 4.1 connects C_{OVP} to V_{SS} to deviate the resonance frequency of L_2C_2 from 13.56 MHz and decrease $V_{IN1,2}$ as well as V_{REC}. Once V_{REC} is reduced, C_{OVP} is disconnected and the L_2C_2 can return back to 13.56 MHz, unless V_{REC} > $V_{threshold}$ condition is persistent. This mechanism regulates V_{REC} around $V_{threshold}$ as long as the input voltage is too high without dissipating extra heat within the rectifier. However, the amount of frequency deviation depends on C_{OVP} value. To cope with larger input voltages, larger C_{OVP} is required. Fig. 4.4 shows the measured V_{REC} vs. V_{L1} for two C_{OVP} values. It can be seen that with the frequency deviation resulted from C_{OVP} = 40 pF, the rectifier can be protected against V_{L1} up to ~60 V, while C_{OVP} = 120 pF can protect the rectifier against V_{L1} up to ~68 V. In practice, V_{L1} is often constant and a sudden reduction in d or I_{REC} activates the OVP circuit.

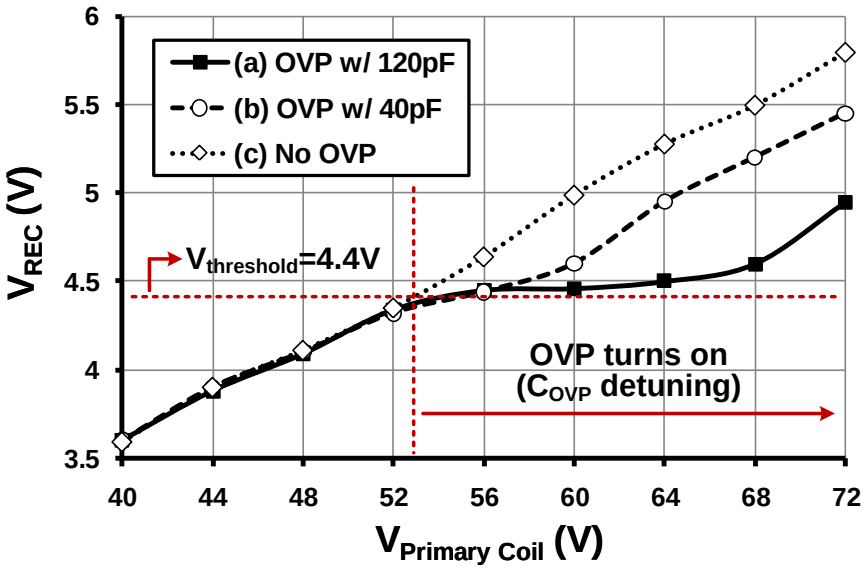


Fig. 4.4. Measured V_{REC} vs. primary coil voltage, V_{L1}, with overvoltage protection (OVP) circuit using C_{OVP} = 120 pF (curve-a), C_{OVP} = 40 pF (curve-b), and without overvoltage protection (curve-c) when R_LC_L = 500 Ω || 10 µF.

4.2. Intraoral Tongue-drive System (iTDS)

4.2.1. Power-management Circuits in iTDS

Tongue drive system (TDS) is a tongue-operated, minimally invasive, unobtrusive, and wireless assistive technology (AT) that infers users' intentions by detecting their voluntary tongue motion, and translating them into user-defined commands. Our GT-bionics lab presented the new intraoral version of the TDS (iTDS), which has been implemented in the form of a dental retainer to read the magnetic field variations inside the mouth from four 3-axial magnetoresistive sensors located at four corners of the iTDS printed circuit board (PCB) [69]. The power-management circuits in the iTDS system-on-a-chip (SoC) provide individually regulated and duty-cycled 1.8 V supplies for sensors, analog front-end (AFE), transmitter (Tx), and digital control blocks, while charging a 50 mAh Li-ion battery with constant current up to 4.2 V and recovering data and clock to update its configuration register through a 13.56 MHz inductive link.

Fig. 4.5 shows the schematic diagram of the power-management circuits in the iTDS SoC including a rectifier, a regulator, a battery charger, a battery monitoring circuit, and bidirectional data telemetry. During normal iTDS operation, the power-management circuits are only in charge of power scheduling and bias generation, thus most of its sub-blocks are off. However, when the iTDS dental retainer is placed inside the charging cup of the TDS universal interface, the 13.56 MHz power carrier couples onto the L_2C_2 tank, generating an AC signal across the full-wave active rectifier inputs, which supplies the rest of the power-management circuits and charges the iTDS embedded 50 mAh Li-ion battery, as shown in Fig. 4.5. The design and operation of the active full-wave rectifier, which offers high AC-to-DC power conversion efficiency (PCE) in the order of 80% at 13.56 MHz thanks to its offset-controlled high speed comparators and optimally sized switches, can be found in chapter 2. The separate low dropout regulators (LDO) provides 1.8 V supply voltages to analog, digital, Tx, and sensor blocks individually to prevent the noise and interference across each block.

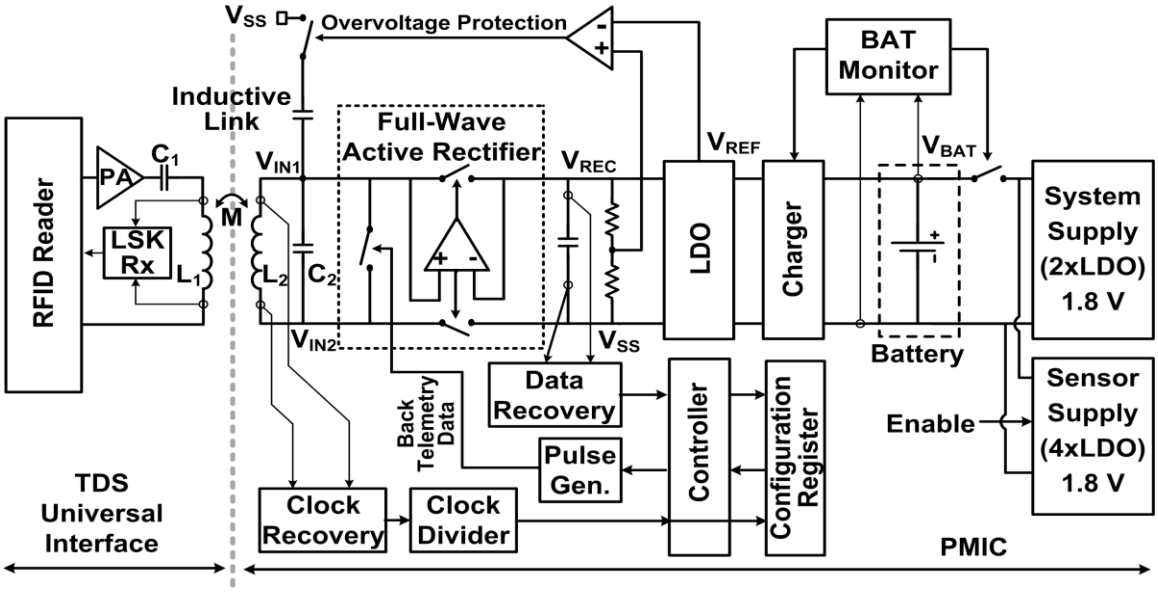


Fig. 4.5. Schematic diagram of the power management IC, including the rectifier, regulator, battery charger, and bidirectional data telemetry.

The power-management circuit has bidirectional data telemetry capability with the RFID reader in the TDS universal interface that drives the inductive link. Fig. 4.6 shows the schematic diagrams of the clock and data recovery circuits for the forward data telemetry. Clock recovery circuit in Fig. 4.6a generates the clock signal by comparing the 13.56 MHz sinusoidal signal across the L_2C_2 tank. The recovered clock is then buffered and divided by 256 to provide a 53 kHz master clock signal for the rest of the system. For data recovery, variations on the V_{REC} due to ASK of the power carrier by the RFID reader are fed into the data recovery circuit in Fig. 4.6b. This simple circuit detects V_{REC} amplitude variations using two paths with different time constants, $R_1C_1 < R_2C_2$, which are connected to a hysteresis comparator. The difference between input node voltages following V_{REC} amplitude transitions results in the recovered forward data bit stream at the output of the comparator, which are sampled and delivered to the configuration register by the back telemetry controller, as shown in Fig. 4.5. This controller also generates a short pulse for every detected bit "1" and applies it to the load-shift-keying (LSK) mechanism of the active rectifier. Shorting the rectifier input results in a sudden

drop in V_{IN} and increased current in L_1. The current and voltage variations in L_1 are detected by the RFID reader and used to recover the LSK back telemetry data.

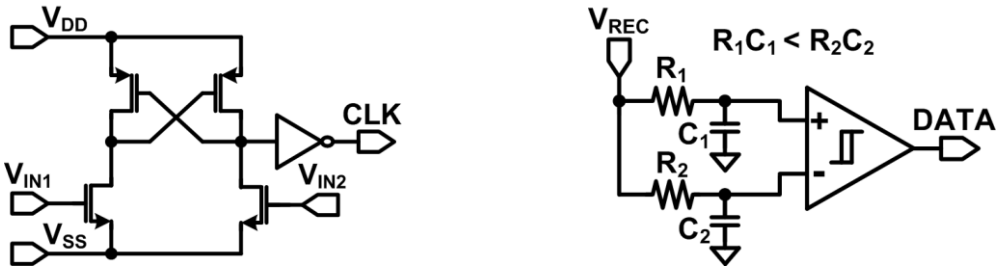


Fig. 4.6. Schematic diagram of (a) clock recovery and (b) ASK data recovery circuits for forward data telemetry.

An LDO after the rectifier provides the Li-ion battery charger with a constant 4.4 V supply. Battery charger provides a constant charging current of 6.8 mA to the battery as long as V_{BAT} < 4.2 V. When V_{BAT} is charged near 4.2 V, the charger switches from constant current to constant voltage mode and keeps V_{BAT} at 4.2 V to continue charging the battery without damaging it [93]. During constant voltage mode, the charging current gradually decreases, until the charger stops charging the battery when the current goes below 5% of its nominal value. Once V_{BAT} reaches its maximum charging voltage of 4.2 V or the inductive link powering is removed, the battery monitoring circuit disables the battery charger operation and connects the battery to the system supply for starting the normal iTDS operation.

The PMIC has been equipped with a detuning-based overvoltage protection circuit, which compares $V_{REC}/4$ with V_{REF}, as shown in Fig. 4.5, and closes a switch that detunes the L_2C_2 tank when V_{REC} is too high. Detuning is a safety measure that results in a considerable drop in V_{IN}, which prevents possible damage to the active rectifier and other circuits when the rectifier output voltage has grown too large as a result of the coils being too close or the load current being too small.

4.2.2. Measurement Results

The iTDS SoC was fabricated in the ON-Semi 0.5-µm 3M2P standard CMOS process, resulting in 3.8 × 3.7 mm^2 chip area. Fig. 4.7 shows the micrograph and floor plan of the chip with emphasis on the power-management circuits.

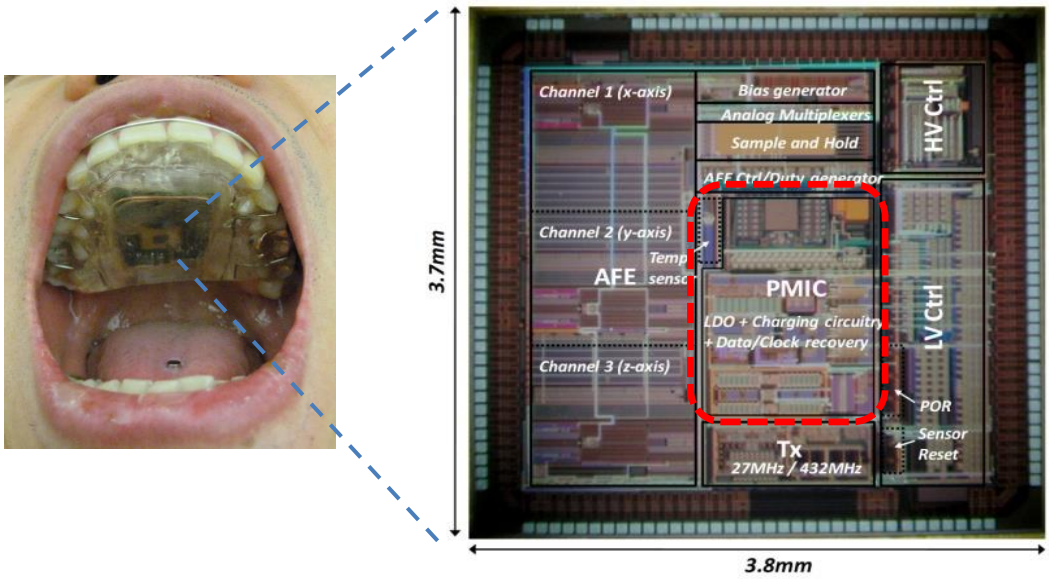
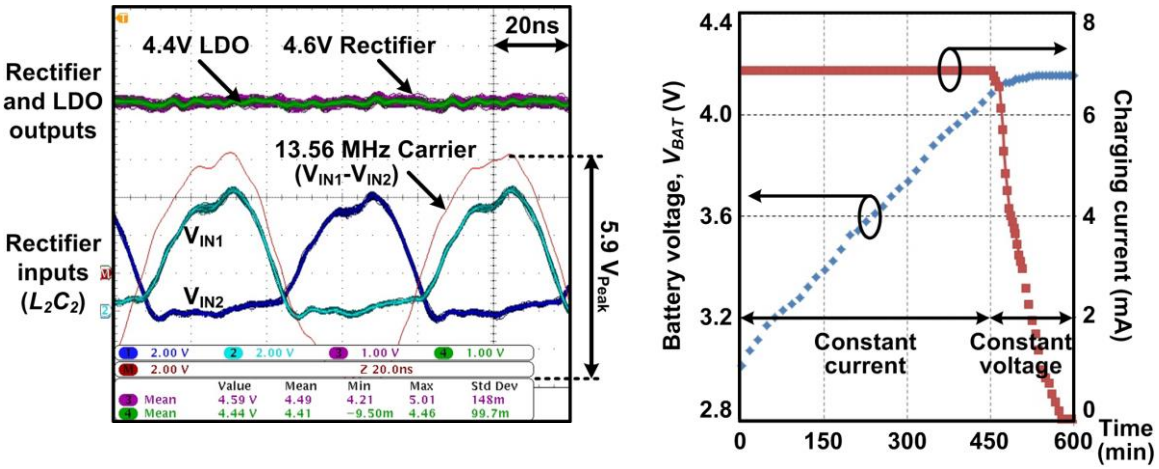


Fig. 4.7. Chip micrograph of the iTDS SoC with emphasis on the power-management circuits.

Fig. 4.8 shows the measured results of the power-management circuit. In Fig. 4.8a, the active rectifier receives 13.56 MHz sinusoidal waveform at V_{IN1} - V_{IN2} = 5.9 V_{peak} from L_2C_2 tank and converts it to 4.6 V DC output. The LDO generates a 4.4 V regulated output that supplies the rest of the power-management circuits. The measured PCE of the active rectifier was ~75% at 6.9 mA load current, 6.8 mA of which was dedicated to the battery charger. Fig. 4.8b shows the battery voltage and the charging current profile. For V_{BAT} < 4.2 V, the battery is charged up at 6.8 mA. When V_{BAT} is nears 4.2 V, the battery charger provides a constant voltage of 4.2 V, while the charging current gradually drops. The 50 mAh Li-ion battery takes ~8 hours to be fully charged through the inductive link.

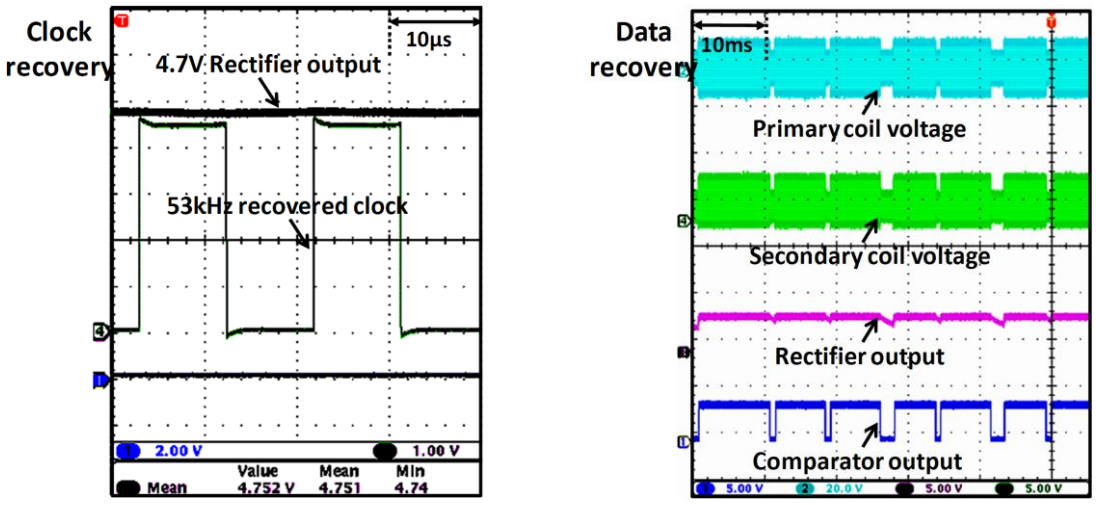
Fig. 4.9 shows the clock and data recovery for the forward data telemetry. In Fig. 4.9a, the clock recovery circuit converts the 13.56 MHz inductive carrier to a 13.56 MHz clock signal, which is divided by 256 to generate the 53 kHz clock signal that is used by

the rest of the iTDS SoC. Fig. 4.9b shows the ASK demodulator waveforms. From top, the 24 V_{pp} sinusoidal voltages across the primary L_1C_1 tank are ASK-modulated by the RFID reader with a modulation index of 33%, which appears across the secondary L_2C_2 tank and V_{REC} on the 2nd and 3rd traces, respectively. Finally, the comparator in Fig. 4.6b recovers the serial data bit stream at 1 kbps on the bottom waveform. The serial data is then oversampled by the clock signal in the controller block and saved in its registers.



(a) (b)

Fig. 4.8. (a) Measured waveforms of the active rectifier and LDO. (b) Li-ion battery inductive charging profile, showing its switching from constant current to constant voltage mode at ~4.2 V.



(a) (b)

Fig. 4.9. Measured waveforms of the (a) clock and (b) the data recovery circuits for the forward telemetry.

CHAPTER V

A COMPACT DISTRIBUTED STIMULATING SYSTEM FOR MULTICHANNEL DEEP BRAIN STIMULATION

5.1. Introduction

Deep brain stimulation (DBS) devices that currently have only 4 stimulating sites and use primary batteries implanted in the chest area, where there is more space available, are moving towards larger number of sites for better current steering capability and elimination of the subcutaneous interconnects that currently pass across the neck to connect the pulse generator to electrodes [50]. To address limitations of the implantable primary batteries, wireless power transmission via inductive links is used in cochlear and retinal implants, which consists of two loosely-coupled coils across the skin and can indefinitely transfer power from an external energy source (battery) directly to the IMD or an implanted rechargeable battery. Moreover, there is demand for increasing the number of stimulation electrodes to improve the accuracy and effectiveness of stimulation. For this feature, high density electrode arrays need to be implemented in small size to be implantable.

In addition, the stimulators need to have the capability of multi-electrode stimulation which can select the desired stimulation channels and provide the stimulation pulses to those specific electrodes. Fig. 1.5 in chapter 1 shows the overall configuration of a multi-electrode DBS system with the proposed method as an exemplar application. The external DBS processor unit, which includes the battery, provides transcutaneous power and data transmission through a pair of coupled coils, *i.e.* the inductive link, across the skin. This part of the system can be designed to be hidden behind the ears (BTE), similar to cochlear implants. The implanted coil generates an AC input voltage, which is provided to the rest of the DBS system with high density electrode array through only two connecting wires, all of which can be embedded inside a DBS lead less than 2 mm in diameter.

Inside the DBS lead, every electrode has its corresponding distributed stimulator application specific integrated circuit (ASIC), which is placed just near each electrode. Only two connections pass through the DBS lead and are connected to each distributed stimulator ASIC in parallel to provide both power and data. Therefore, each distributed stimulator ASIC can be activated to provide the proper stimulation pulses to its electrode by sharing those two connecting wires from the implanted coil. With this feature, a high density DBS lead, with for example 64 electrodes, can be implemented in a smaller size with only two connecting wires passing through the lead and performing the multi-electrode stimulation with directionality for targeting the desired neural tissues by generating the stimulation pulses to the selected electrodes.

5.2. System Architecture

In the conventional DBS system, a large number of connecting wires between the DBS electrodes and the central stimulator IMD significantly limit the possibility of minimizing the implantable DBS lead size, leading to safety issues on mechanical connections especially when the number of electrodes increases. Fig. 5.1 shows the block diagram of the 64-channel DBS system with the conventional method, as an example. The central stimulation IMD needs to have 64 outputs each of which is wired to a stimulation electrode all through the cylindrical DBS lead. The large number of wires (64 in this case) from the stimulator IMD to each stimulation electrode affects the diameter of the DBS lead significantly, which is quite size-constraint to minimize damage to the neural tissue when implanted [72]. The volume of the connecting wires has become a critical factor that restricts the number of stimulation electrodes in the traditional architecture. In addition, using many connecting wires can make the lead too stiff and inflexible. Creating a bundle of wires that is not too thick would require the individual strands of wires to be very thin. Using very thin wires makes them mechanically unreliable and increases the possibility of failure in presence of mechanical stress during

the implantation surgery or regular usage. Moreover, using thin wires increases the resistivity of interconnects that should deliver the stimulation current from the pulse generator to the stimulating sites, resulting in larger dropout voltage, heat dissipation, and requirement for higher back end stimulation voltage.

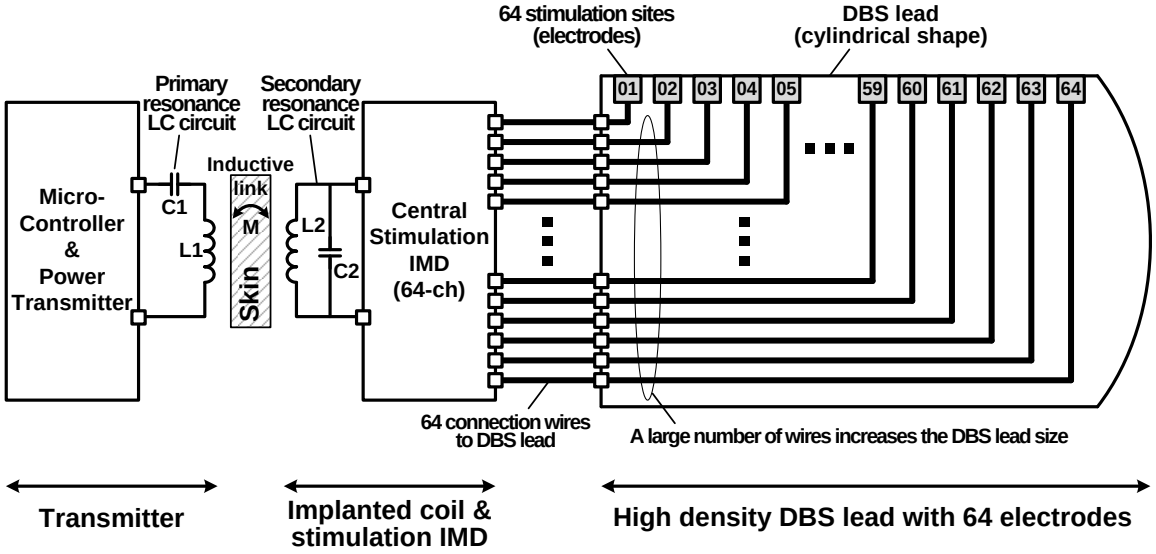


Fig. 5.1. Simplified block diagram of the 64-channel DBS system with a conventional architecture.

Liu *et al.* recently proposed the design of an implantable stimulator that minimizes cable count using ASICs close to the electrodes [73]. In this method, each stimulator ASIC is located near its stimulation electrode and shares four input lines, two supply voltages and two clock signals, from the hub to reduce the connecting wire count. However, each stimulator IC still requires one separate input line for the bidirectional communication from the hub. Thus the connecting wire count for N stimulation electrodes would be N+4, which is proportional to the number of stimulation electrodes, and the stimulator still suffers from the large volume of connecting wires when a large number of electrodes are required for stimulation.

Ibrahim *et al.* has proposed a multi-electrode cochlear system with distributed electronics, in which digital circuits (decoders and switches) are placed near the electrodes to perform multiplexing leading to a reduction in the required number of

interconnecting wires [74]. However, this method requires at least 6 connecting wires, two of which are for stimulation output pulses, two for electrode selection data and clock, and two for supply voltages. Therefore, the volume of connecting wires still limits the size of the stimulation system for IMD applications. Moreover, passing DC voltage inside the body is not safe due to the possibility of leakage and electrolysis of water.

Similarly, Duncan *et al*. also proposed a distributed functional electrical stimulation system in which distributors are located near each stimulation site for stimulating a plurality of different sites with a central implantable stimulator unit [75]. The distributor, which consists of the control logic, power storage, and switch element blocks, requires at least three connecting wires, two of which are the stimulation output pulse and the ground voltage, and the other is the control signal. However, the power storage block is implemented with a quite large capacitor, which is charged through the control signal from the central stimulator unit, or a battery, which requires an individual inductive link for recharging. Both of them significantly increase the size of the distributors which are not suitable for the implantable devices.

Andreu *et al.* also introduced a distributed architecture for peripheral nerve stimulation, in which the distributed stimulation units, including the stimulation pulse generator and the digital block, are located near their corresponding electrodes and drive them with stimulation pulses [76]. These distributed stimulation units receive two wires in parallel from the central controller for communication, but they also require at least two more wires or internal batteries to receive power. In addition, the current 4-electrode DBS lead (e.g. model 3387 from Medtronic) consists of cylindrical stimulating sites that are ~1.27 mm in diameter and 1.5 mm in length, while Andreu's distributed stimulation units occupied much larger silicon area of 22 mm^2, which may suit peripheral nerve stimulation but not be suitable for the multi-electrode DBS or cochlear applications.

Gerber *et al.* proposed a neuro-stimulation system with distributed stimulators which receives the data wirelessly from the main controller unit [77]. However, the

distributed stimulator requires the receiver block for the data communication, which consumes quite large power. Moreover, each distributed stimulator operates with its own internal battery, which is not suitable for the size-constraint applications such as the DBS or the cochlear implants.

With the proposed distributed stimulating method, the circuitry inside the central stimulation IMD can be modified and moved into the DBS lead, and the number of connecting wires can be significantly reduced from the number of electrodes to only two regardless of the number of electrodes. This will lead to the implantable DBS lead to have small diameter, particularly for high density electrodes. In this new architecture, power and data are transferred wirelessly through an inductive link without using internal batteries, which were usually located in the chest area due to their large volume. The implanted coil, on the other hand, can be moved near the DBS lead on the head, thanks to its small size, similar to a cochlear implant, with the main controller and energy source remaining outside the body in the form of a BTE device.

Fig. 5.2 shows the 64-channel DBS system with the proposed distributed stimulator method as opposed to the conventional method in Fig. 5.1. The overall operation of the proposed distributed stimulator method is as follow. The external power transmitter drives the primary coil, L_1, at the power carrier frequency. The signal is induced on to the secondary coil, L_2, through the inductive link, and generates an AC voltage across the resonance circuit, L_2 and C_2. Then, these AC input voltages, V_{COIL} and *GND*, are provided to the DBS lead through two input wires and connected to each distributed stimulator IC in parallel. Therefore, the number of wires, which goes through the DBS lead, is only two and independent to the number of stimulation electrodes allowing smaller diameter of the implantable DBS lead for the multi-electrode stimulation. With the two input wires, V_{COIL} and *GND*, the distributed stimulator ICs are capable of generating the power to simulate the electrodes as well as performing the bidirectional data communication to set up the stimulation parameters and activate the

stimulation channels. Therefore, the distributed stimulator system has only two connecting wires regardless of the number of stimulation electrodes, which allows the small-sized multi-electrode stimulation systems to be easily implantable with minimum damage to the surrounding neural tissue.

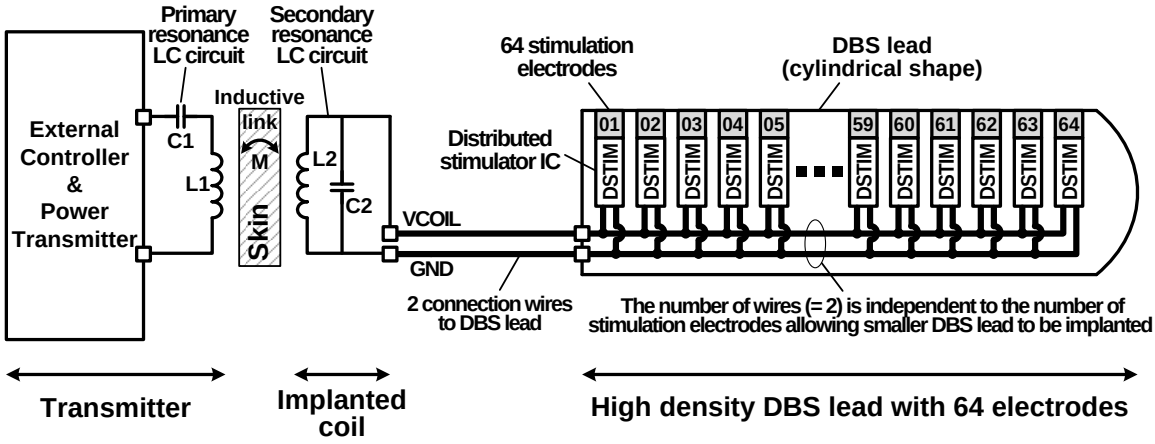


Fig. 5.2. Simplified block diagram of the 64-channel DBS system with the proposed structure using distributed stimulator ASICs next to each stimulation electrode.

5.3. Circuit Design and Implementation Details

The detailed block diagram of the distributed stimulator IC is presented in Fig. 5.3. It consists of four main blocks which are the power management IC (PMIC), the stimulator (STIM), the forward telemetry, and the back telemetry. In the PMIC, the AC-to-DC converter receives the AC input voltages, V_{COIL} and *GND*, and converts them to the DC voltage, which is regulated through the low dropout regulator (LDO) and then supplies the rest of the ASICs. For the forward telemetry, the external power transmitter sends the modulated signals, which also make V_{COIL} modulated. The demodulator circuit detects the variations of V_{COIL} and generates the demodulated digital signals, which are then divided into synchronized clock and data through the clock and data recovery (CDR). The serial-to-parallel (S2P) converter stores the data to the configuration registers to generate the stimulation timing signal through the timing control block and adjust the

stimulation parameters. Several modulation techniques can be adopted for the forward telemetry such as amplitude-shift-keying (ASK), frequency-shift-keying (FSK), phase-shift-keying (PSK), and on-off-keying (OOK) [78]. The stimulator block, which is a single-channel stimulator, provides the stimulation pulses to the designated stimulation electrode according to the settings through the forward data telemetry.

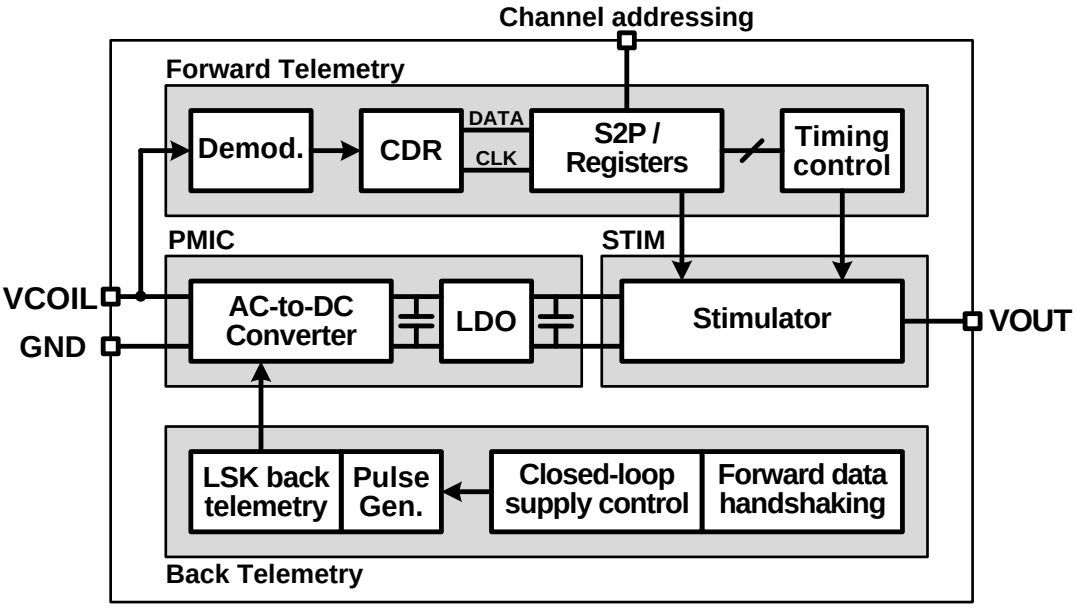


Fig. 5.3. Block diagram of the distributed stimulator ASIC.

The back telemetry can be also utilized through the two input voltage lines by using the load-shift-keying (LSK) modulation [30]. In order to send the back telemetry signal to the external micro-controller, the LSK back telemetry circuit makes two input lines shorted together or disconnected to the AC-to-DC converter for a short time to lead the load impedance variation. For example, when two input lines are shorted together, it results in a sudden drop in the voltage across L_2 and increased current in L_1, which also increases the voltage across L_1. Current and voltage variations in L_1 are detected by the external micro-controller and ASK-demodulated to recover the LSK back telemetry data. This back telemetry can be used for several purposes such as the closed-loop power control to make the supply voltage constant against the coil voltage variations or the

handshaking signal to confirm the proper data transmission through the forward telemetry. Each distributed stimulator ASIC has channel addressing bits to distinguish the stimulation channels which the users want to activate.

In order to receive the power from the shared two input lines, several AC-to-DC converter structures can be used in the distributed stimulator IC. Fig. 5.4 shows the examples of available AC-to-DC converters in the distributed stimulator IC and their configurations. In Fig. 5.4a, the AC-to-DC converter is replaced with a rectifier in which a diode and a filtering capacitor convert the AC input voltage, V_{COIL} - *GND*, to the DC supply voltage. In Fig. 5.4b, the voltage doubler was used as the AC-to-DC converter. The voltage doubler can generate the desired DC output voltage with smaller AC input voltage, which can extend the inductive power transmission range. The voltage doubler input capacitor, C_3, located after the secondary *LC* circuit, can be shared by all distributed stimulator ICs. Therefore, using voltage doubler does not increase the number of off-chip capacitors required in the distributed stimulator ASIC compared to using the rectifier.

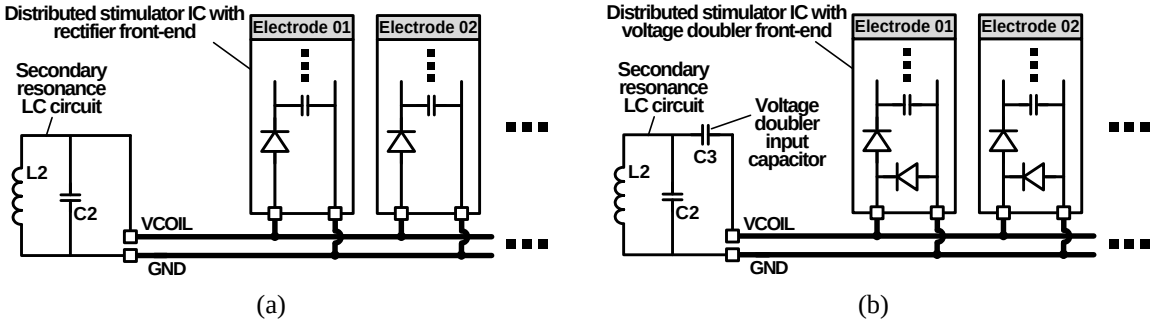


Fig. 5.4. Available AC-to-DC converter blocks in the distributed stimulator ASIC and their configurations: (a) the distributed stimulator ASIC with a rectifier front-end and (b) the distributed stimulator ASIC with a voltage doubler front-end.

Fig. 5.5 shows the 64-channel DBS lead and its cross-section view as an implementation example of the distributed stimulator method. As explained, only two input lines, V_{COIL} and *GND*, go through the DBS lead and are connected to input pads of the distributed stimulator ASIC for providing both power and data to each distributed stimulator IC, minimizing the diameter of the DBS lead that is suitable for the

implantable multi-electrode stimulation. The distributed stimulator IC can be fabricated with a small area less than a few millimeters square. In order to regulate the AC-to-DC converter and LDO output voltages, the distributed stimulator ASIC also requires two off-chip capacitors, for which a small-sized commercial capacitors (*e.g.* 0201-size capacitor with 0.6 mm length, 0.3 mm width, and 0.3 mm height) are available. Therefore, placing the distributed stimulator ASIC closed to its electrodes and connecting two shared input lines to the input pads of every distributed stimulator ASIC in parallel are practical to be implemented with current technologies.

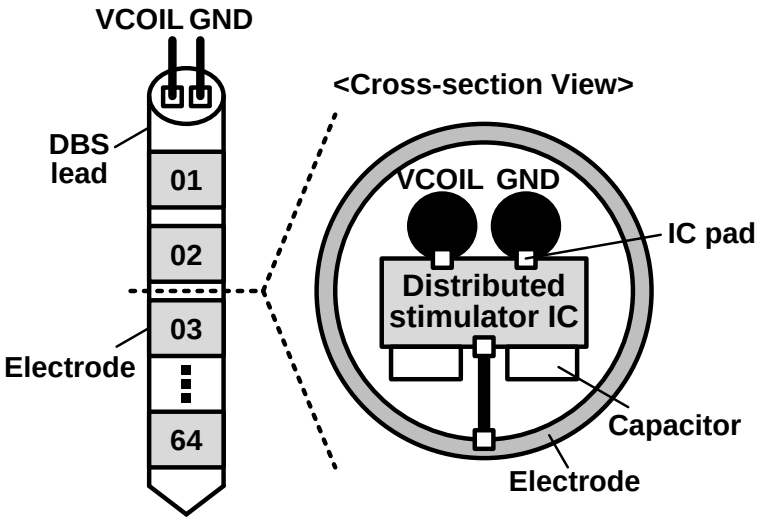


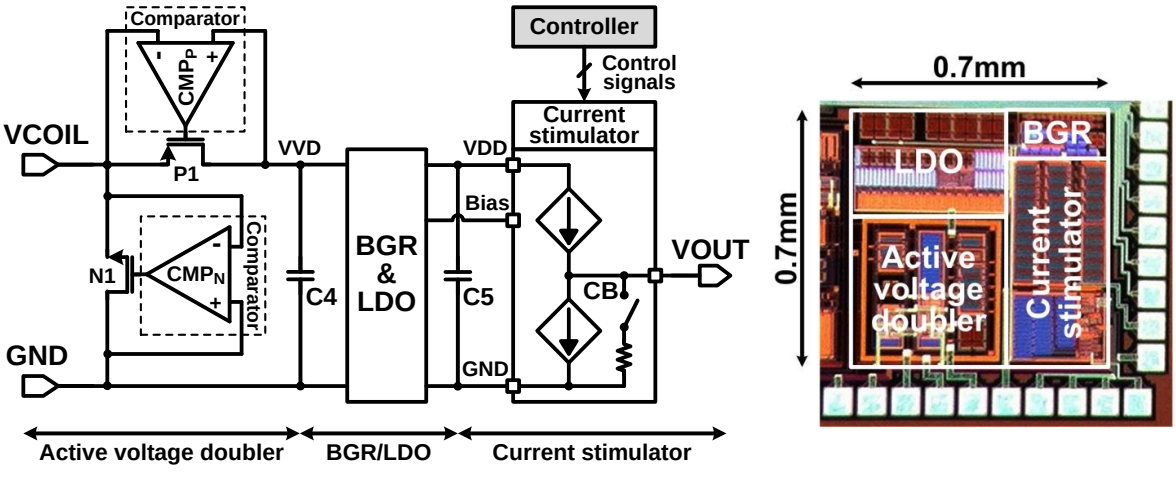
Fig. 5.5. Example of the 64-channel DBS system implementation and the cross-section view of the DBS lead with the proposed distributed stimulator ASICs.

5.4. Measurement Results

5.4.1. Prototype Distributed Stimulator and Test Setup

In order to verify the operation of the multi-electrode stimulation system with distributed stimulators, we implemented a prototype system with four distributed stimulator ASICs on a prototype printed circuit board (PCB). The prototype distributed stimulator ASICs only included the PMIC and the stimulator blocks in Fig. 5.3. The stimulation parameters and timing signals were provided by a commercial microcontroller (nRF24LE1, Nordic Semiconductor).

Fig. 5.6a shows the conceptual block diagram of the prototype distributed stimulator ASIC including the active voltage doubler, bandgap reference (BGR), LDO, and current stimulator. In this prototype distributed stimulator, a comparator-based active voltage doubler block was adopted as the AC-to-DC converter, which configuration is shown in Fig. 5.4b. The secondary resonance circuit, L_2C_2 tank, and the voltage doubler input capacitor, C_3, generate two shared input voltage nodes, V_{COIL} and *GND*, which are provided to all distributed stimulator ASICs in parallel via their two input lines. The active voltage doubler converts the AC input voltage to DC output, V_{VD}, by turning on rectifying switches, P_1 and N_1, at proper times with high speed comparators, CMP_P and CMP_N, respectively. BGR and LDO blocks generate the regulated supply, V_{DD}, and the bias voltages. The voltage doubler and LDO have output filtering capacitors, C_4 and C_5, respectively, which are off-chip components. The current stimulator ASIC provides the push or pull current stimulus depending on the control signals from the external microcontroller chip. The CB switch was utilized for passive charge balancing after stimulation. Fig. 5.6b shows the fabricated chip micrograph of the distributed stimulator ASIC occupying 0.49 mm^2.



(a) (b)

Fig. 5.6. (a) Simplified block diagram of the prototype distributed stimulator ASIC including the active voltage doubler, BGR, LDO, and current stimulator. (b) Fabricated distributed stimulator chip micrograph.

Fig. 5.7 shows the test setup for a 4-channel distributed stimulating system for DBS that is made up of 4 distributed stimulating ASICs and a commercial microcontroller chip (nRF24LE1). The external power transmitter board induces the AC power at 13.56 MHz across the L_2C_2 tank, as shown in Fig. 5.2, to all distributed stimulator ASICs through the inductive link, L_1 and L_2. Two out of four distributed stimulator channels are selected to provide the biphasic stimulation current to the load, which stimulation parameters, such as amplitude, pulse width, and inter-phase delay, are controlled by the microcontroller chip.

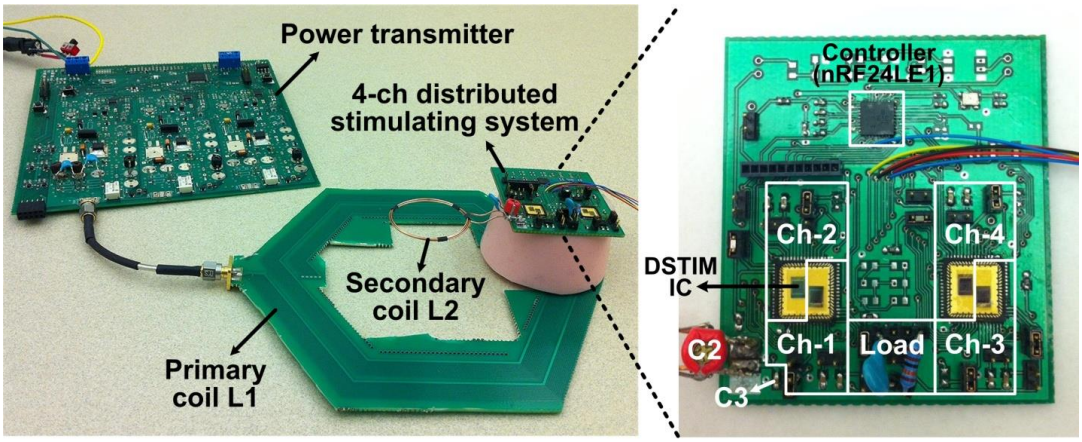


Fig. 5.7. Test setup of the 4-channel distributed stimulating system with four prototype distributed stimulator ASICs and a commercial microcontroller (nRF24LE1).

5.4.2. Distributed Stimulation Waveforms

Fig. 5.8 shows the measured waveforms focusing on supplying power to each distributed stimulator ASIC. Through the inductive link, the secondary resonance circuit, L_2 and C_2, generates 2.3V peak-to-peak AC voltage across it, and the AC voltage is level-shifted through C_3 and the diodes of the voltage doublers, generating two input voltages, V_{COIL} and *GND*. By sharing these two input lines, all four distributed stimulator ICs can generate the same voltage doubler output voltages of 4 V, which are sufficient to supply the rest of the ASIC after regulation. The distributed stimulator ASIC consumes a relatively large dynamic power only when it is selected for providing the stimulation

pulses. All the other distributed stimulator ASICs, which are not activated, consume only a small static power. As such, the external part of the system and inductive link become capable of providing sufficient power to a large number of distributed stimulator ASICs, *e.g.* 64 channels or more, through the inductive link as long as a small number of channels are activated for stimulation while the others are kept in the standby mode to consume negligible power.

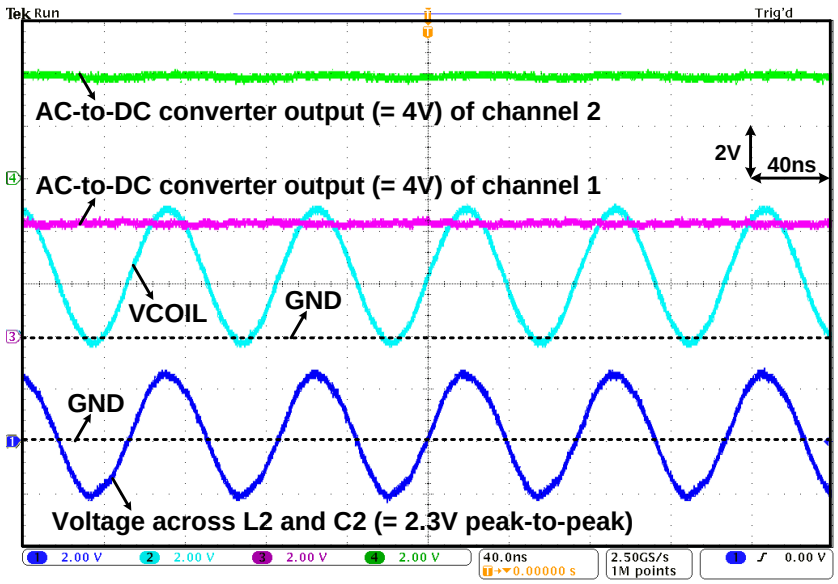


Fig. 5.8. Measured waveforms focusing on the power delivery from the secondary resonance circuit, L_2C_2 tank, to each distributed stimulator ASIC.

Fig. 5.9 shows the measured waveforms focusing on multi-electrode stimulation. Among four channels, channel 1 and 2 were selected for stimulation, and the other channels were in the standby mode. For the first stimulation phase, channel 1 pulls the stimulation current while channel 2 pushes the stimulation current, leading to a stimulation voltage across the load (R = 1.3 kΩ and C = 100 nF in series) with negative polarity. Then, after a programmable inter-phase delay period, a positive polarity stimulation voltage is applied across the load during the second stimulation phase. Fig. 5.10 shows the same measured waveforms in Fig. 5.9 with a longer time scale to verify

that the selected distributed stimulation ASICs can provide the desired stimulation pulses properly over time.

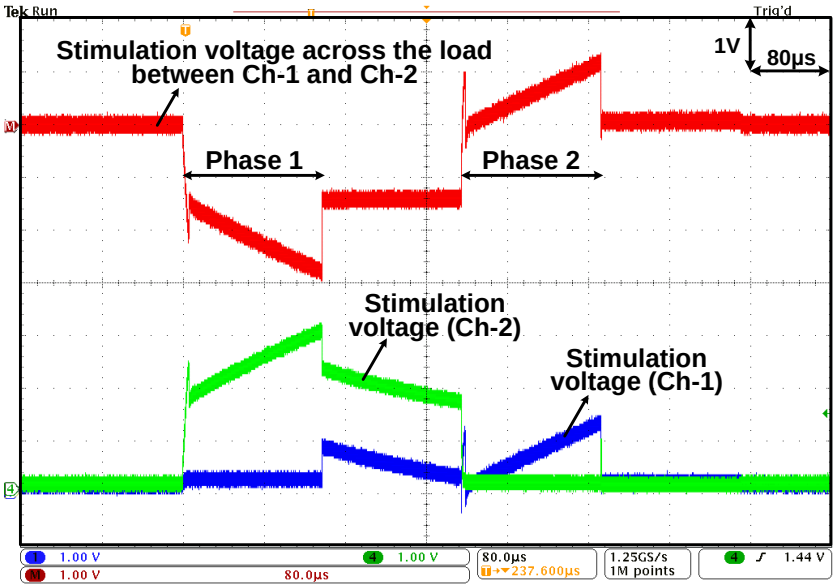


Fig. 5.9. Measured waveforms focusing on the multi-electrode stimulation.

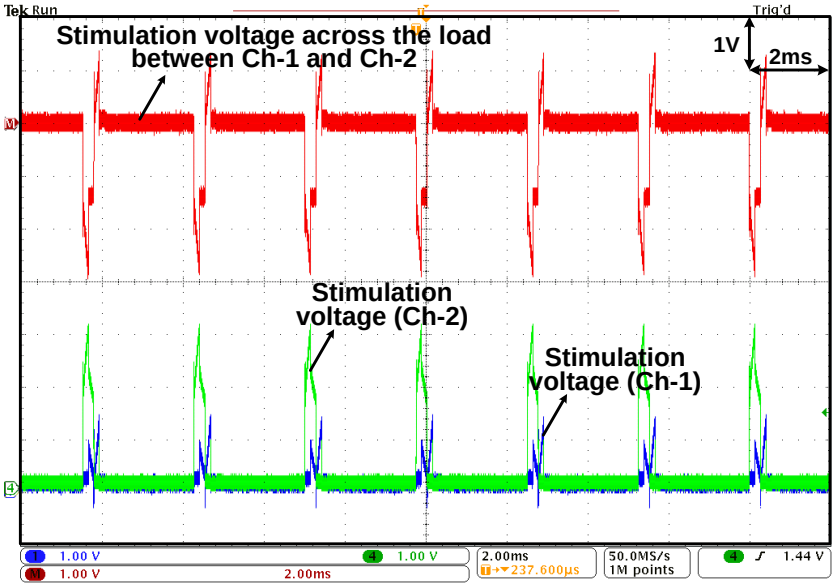


Fig. 5.10. Measured waveforms focusing on the multi-electrode stimulation with longer time scale.

In addition, we have fabricated an improved distributed stimulating system in TSMC 0.35-µm standard CMOS process. The fully on-chip distributed stimulator IC module includes a power-management block, current stimulator, and forward/back

telemetry as shown in Fig. 5.3. The fabricated distributed stimulator IC with floor planning of each block is shown in Fig. 5.11, occupying only 2.4 mm × 1.1 mm, which can be placed near each electrode for distributed stimulating function. Full characterization of the distributed stimulator IC is our future plan. The overall distributed stimulating system will be also verified by connecting several IC modules in series through two input wires as shown in Fig. 5.2.

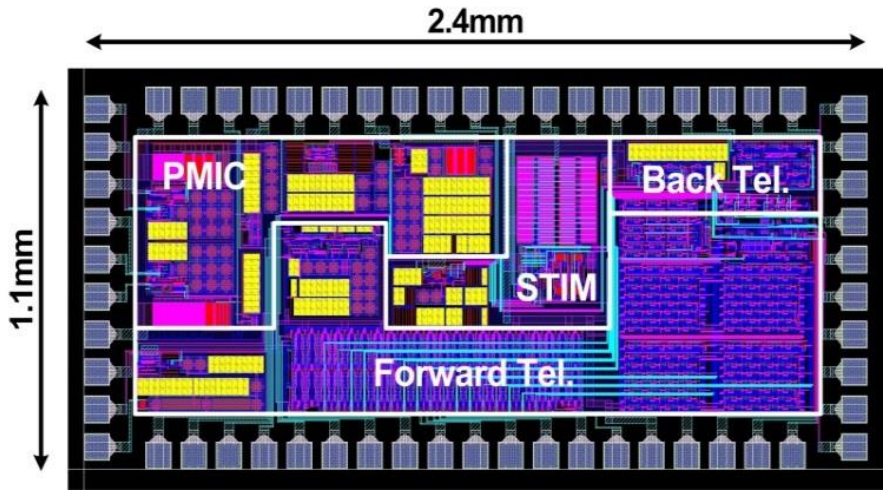


Fig. 5.11. Layout of the distributed stimulator IC occupying 2.4 mm × 1.1 mm.

CHAPTER VI

AN ADAPTIVE WIRELESS NEURAL STIMULATING SYSTEM WITH CLOSED-LOOP SUPPLY CONTROL

6.1. Introduction

Current-controlled stimulators (CCS) have been widely used in implantable electrical stimulators because of their precise current control and safe operation. However, CCS suffers from low power efficiency, which mainly results from the large voltage drop across the output current sources, especially when the necessary stimulation voltage is much smaller than the supply voltage [52], [53]. In order to achieve both safe and power efficient stimulation, we chose CCS with adaptive supply control, *i.e.* the stimulator supply voltage is automatically adjusted near the required stimulation voltage by detecting the site potential and forming a closed control loop through a power-efficient adaptive rectifier. This mechanism minimizes the voltage drop across the current sources, resulting in high power efficiency in the CCS. Our stimulating system also adopts active charge balancing by sharing the closed-loop path of the adaptive supply control to inject small current pulses in the tissue to keep the residual charges within a safe limit. The proposed wireless stimulating system can be utilized for the head-mounted deep brain stimulation (DBS), as shown in Fig. 1.5, in which power and data are transferred through the inductive link while high stimulator efficiency is strongly required to provide a wide range of stimulus to the target brain area without tissue damage from overheating.

6.2. Wireless Stimulating System Architecture

Fig. 6.1 shows the conceptual diagram of the proposed inductively powered wireless stimulating system with the adaptive rectifier and internal closed-loop supply control. In the proposed inductively powered stimulator, the adaptive rectifier with active switching is capable of generating a multilevel DC voltage, V_{REC}, directly from the AC input voltage across L_2 through an internal closed loop control mechanism. Adjusting

V_{REC} changes the power consumption in the IMD, leading to Tx output power variation. Therefore, V_{REC}, which directly supplies the CCS without an LDO, is adaptively adjusted close to the peak of V_{STIM}, resulting in small loss while benefiting from the advantages of the CCS. Moreover, the adaptive rectifier achieves high AC-DC power conversion efficiency (PCE) by adopting the phase control feedback and active synchronous rectification to improve the overall power efficiency of the inductively powered stimulator. The proposed stimulating system in Fig. 6.1 can be compared with various state-of-the-art stimulating structures which are described in chapter 1.2 with Fig. 1.6.

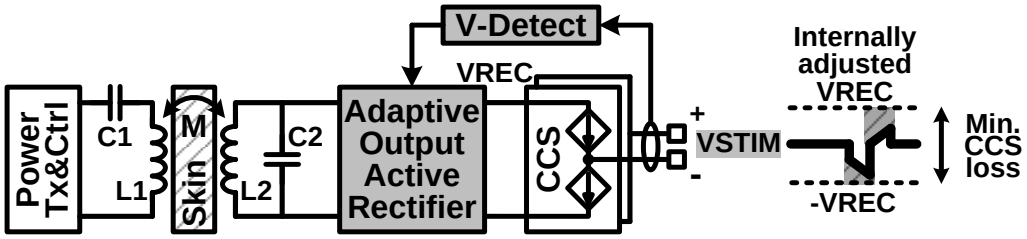


Fig. 6.1. Conceptual diagram of the proposed inductively powered wireless stimulating system with the adaptive rectifier and internal closed loop supply control.

The overall architecture of the proposed inductively- powered head-mounted DBS system is shown in Fig. 6.2. The power management block receives AC input through the inductive link, and converts it to the adjustable V_{REC} depending on the rectifier phase control bits, which are defined by the peak voltage at the stimulation sites that set V_{REF} through the 3-bit resistor DAC (RDAC). The LDO generates the digital supply voltage, V_{DIG}, for the low voltage digital blocks. The overvoltage protection (OVP) circuit monitors the peak of $V_{INP,N}$ and connects a detuning capacitor across the AC input to suppress AC voltages larger than a certain limit.

Two stimulus current drivers, CCS_1 and CCS_2, which are adaptively supplied from V_{REC}, drive four stimulating sites in a complementary fashion with high compliance voltage, increasing the stimulation power efficiency. The voltage readout channel reports the relative voltage difference between active sites to the off-chip microcontroller (MCU),

closing the feedback loop that adjusts V_{REC}. The same loop also manages active charge balancing via on-chip controllers, which inject additional current pulses into the tissue to bring the voltage difference between sites within a certain limit to guarantee safe stimulation. Forward data from the external Tx coil is recovered via amplitude-shift-keying (ASK) demodulation, setting the stimulation parameters and active channels. The back telemetry link utilizes LSK modulation by closing the short-coil (SC) switches across *L2*.

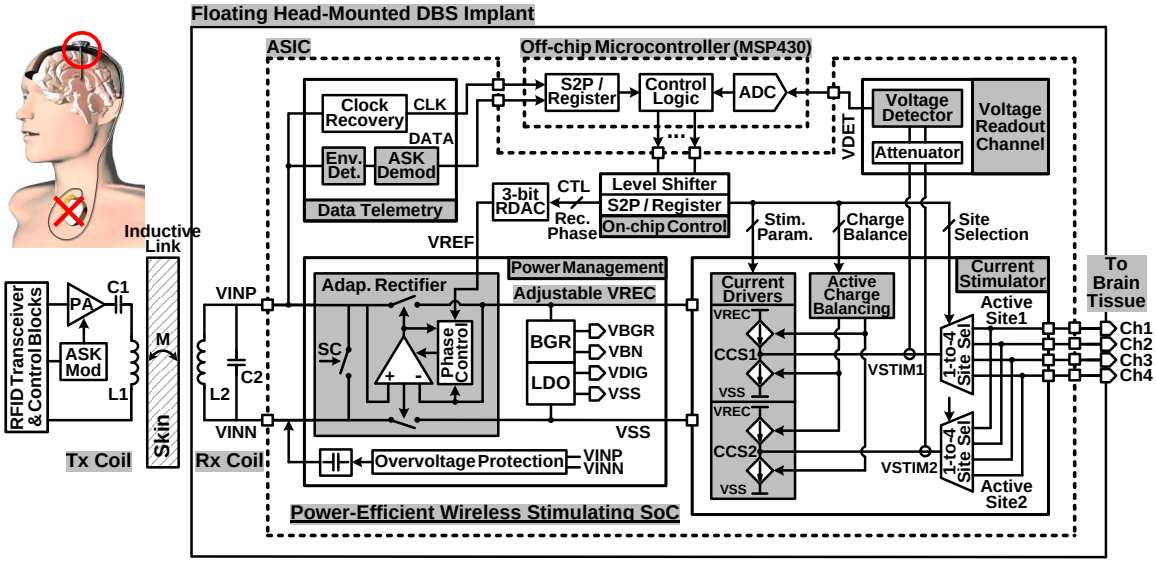


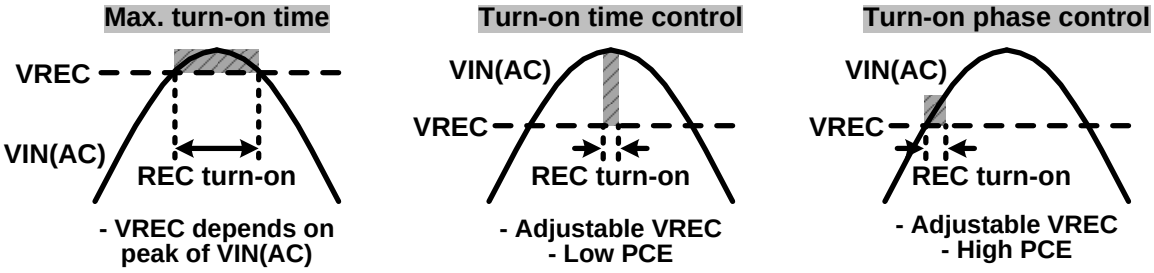
Fig. 6.2. Overall architecture of the proposed inductively powered head-mounted DBS system equipped with the adaptive supply control and the active charge balancing for both power-efficient and safe current stimulation.

6.3. Adaptive Rectifier with Phase Control Feedback

6.3.1. Rectifier Phase Control

In order for the adaptive rectifier to generate the desired multilevel V_{REC}, the rectifier turn-on time needs to be adjusted to limit the forward current, while achieving high PCE. Fig. 6.3 shows the simplified voltage waveforms of the rectifier depending on the turn-on time. Conventional rectifiers aim to generate the maximum V_{REC} from $V_{IN(AC)}$ at high PCE. Therefore, they turn on as long as $V_{IN(AC)} > V_{REC}$, as shown in Fig. 6.3a.

Consequently, V_{REC} becomes dependent on the $V_{IN(AC)}$ amplitude, and it is not internally adjustable. In Fig. 6.3b, V_{REC} can be adjusted by controlling the turn-on time around the peak of $V_{IN(AC)}$. If the turn-on period is reduced, the lower forward current reduces V_{REC} as well. However, the large voltage drop between $V_{IN(AC)}$ and V_{REC} during the turn-on period results in large power loss across the rectifying transistors, resulting in low PCE.



(a) (b) (c)

Fig. 6.3. Simplified voltage waveforms of the rectifier with (a) the maximum turn-on time, (b) the turn-on time control, and (c) the turn-on phase control.

To adjust V_{REC} while maintaining high PCE, we controlled the rectifier turn-on phase as shown in Fig. 6.3c. In this method, the rectifier turns on when $V_{IN(AC)} > V_{REC}$, similar to the conventional rectifiers. However, its turn-off timing is controlled to limit the forward current. Therefore, V_{REC} is adjustable depending on the rectifier turn-on phase, while the small dropout voltage between $V_{IN(AC)}$ and V_{REC} during the on period provides high PCE.

Fig. 6.4 shows the adaptive rectifier feedback model with the phase control mechanism. The threshold crossing detector sends a turn-on signal at phase θ to the synchronous rectifier when $V_{IN(AC)} > V_{REC(DC)}$ to initiate the forward conduction. The phase control feedback compares $V_{REC(DC)}/3$ with a reference voltage, V_{REF}, which indicates the desired V_{REC} level, and generates an error signal, e, that is amplified and converted to a time delay, T_D. T_D is then applied to the turn-on signal at phase θ to generate the delayed signal at phase θ_D using which the turn-off controller turns the rectifier off after T_D. In other words, the rectifier conducts for T_D from the onset of $V_{IN(AC)}$

> $V_{REC(DC)}$ at the turn-on phase of θ to adjust V_{REC}, as shown in Fig. 6.3c.

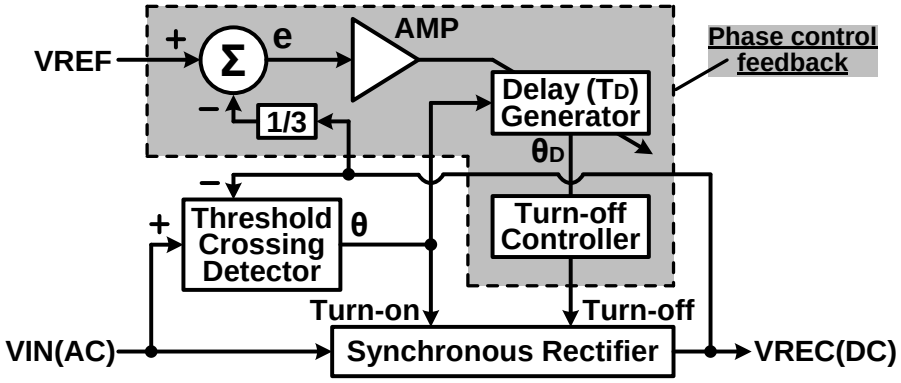


Fig. 6.4. Adaptive rectifier feedback model showing the phase control mechanism.

6.3.2. Implementation of the Adaptive Rectifier

Fig. 6.5 shows the schematic diagrams of the adaptive rectifier with active switches and one of its phase control comparators. In Fig. 6.5a, a pair of comparators, CMP_1 and CMP_2, which are equipped with the phase control feedback, drives the rectifying switches, P_1 and P_2, respectively, for low dropout voltage and high PCE. The reference voltage, V_{REF}, which is provided through a 3-bit RDAC, controls the transition times of the comparator output voltages, V_{O1} and V_{O2}, in a way that the rectifier turn-off timing can be adjusted to change the turn-on phase and consequently the V_{REC} level. P_1 and P_2 turn on alternatively depending on $V_{INP,N}$ polarity, while a cross-coupled NMOS pair, N_1 and N_2, closes the rectifier current path. PMOS body terminals, V_{B1} and V_{B2}, are connected to the highest potential among $V_{INP,N}$ and V_{REC} with the dynamic body biasing circuit [18].

In the phase control comparator (CMP_1), shown in Fig. 6.5b, P_4, P_5, N_6, N_7, P_8, and N_8 form a common-gate comparator with input voltages, V_{REC} and V_{INP}, while the current source, P_7, injects additional current when V_{O1} is high and P_6 turns on, forcing V_1 to increase earlier and expedite the turn-on transition of P_1. The phase control feedback loop consists of inverter chains along with the current-starved inverter, INV_6 and N_{10}, which bias current is controlled through AMP_1 by comparing $V_{REC}/3$ and V_{REF}, to

generate the corresponding time delay. INV_6 output is further delayed before affecting the turn-off control transistor, P_3, which forces the rectifier to turn off adaptively even before $V_{INP} < V_{REC}$ to generate the desired V_{REC}. Therefore, unlike conventional rectifiers or voltage doublers in chapter 2, which output levels are dependent on the $V_{INP,N}$ amplitude, the adaptive rectifier is capable of generating variable supply voltages regardless of the $V_{INP,N}$ amplitude, thanks to the phase control feedback.

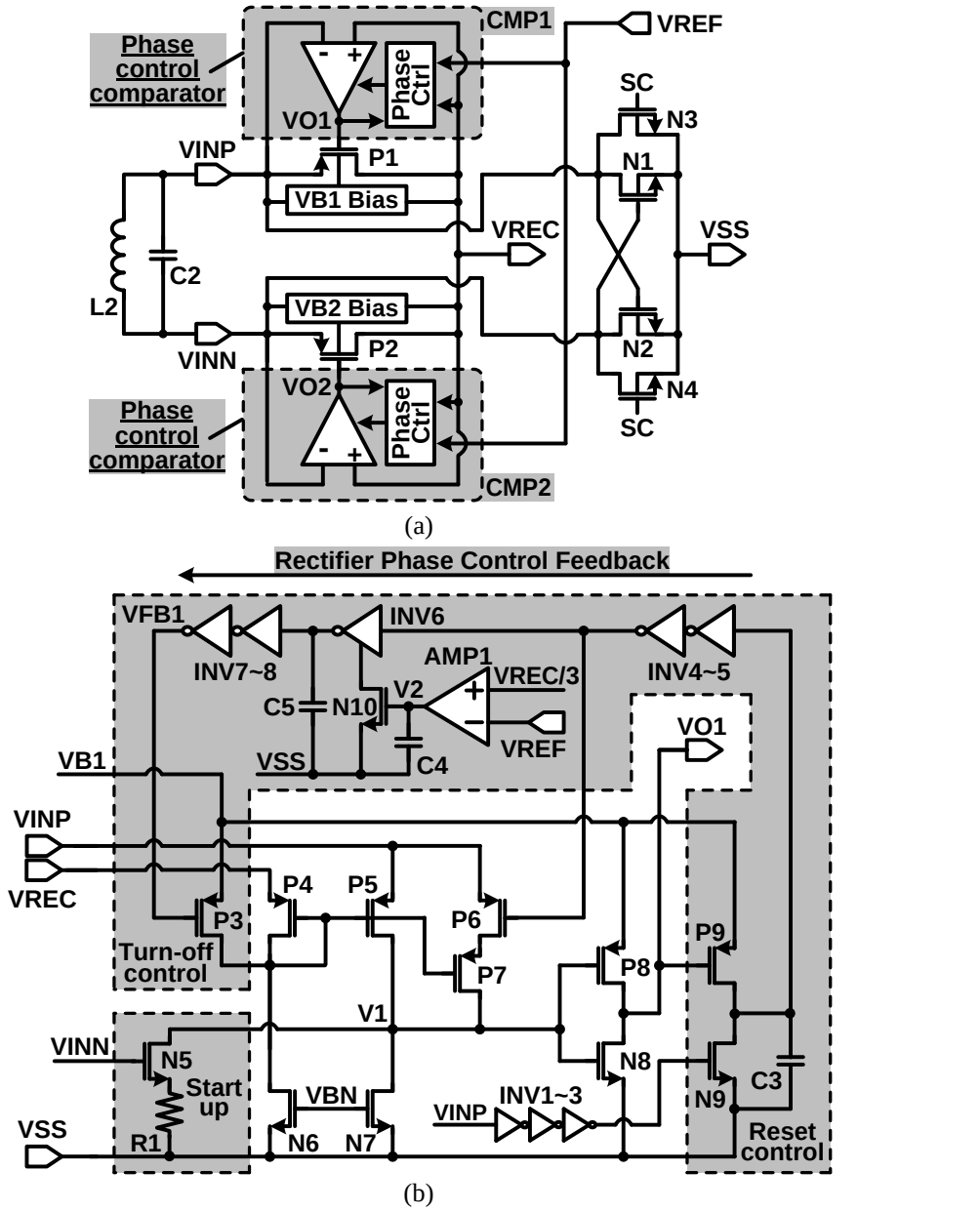


Fig. 6.5. Schematic diagrams of (a) the proposed adaptive rectifier with active switches, and (b) one of its phase control comparators, CMP_1.

Fig. 6.6 shows the timing diagram of the adaptive rectifier depending on the actual V_{REC} level vs. the target V_{REC}, which is $3 \times V_{REF}$. For example, when $V_{REC} > 3V_{REF}$ in Fig. 6.6a, AMP_1 increases V_2, decreasing the delay of INV_6. Once V_{O1} drops to turn on the rectifier, P_3 also turns on by V_{FB1} after a small delay, T_D, limiting the charging period of the load and decreasing V_{REC}. On the other hand, when $V_{REC} < 3V_{REF}$ in Fig. 6.6b, the delay of INV_6 increases as V_2 decreases, and P_3 turns on after a longer T_D or even remains off, allowing more forward current to increase V_{REC}. When $V_{REC} = 3V_{REF}$ in Fig. 6.6c, V_2 results in a T_D that can maintain V_{REC} at the desired value. Since the turn-off timing is controlled in every rectifier cycle, the ripple on V_{REC} can be reduced to that of conventional rectifiers once it is settled on the desired V_{REC} value.

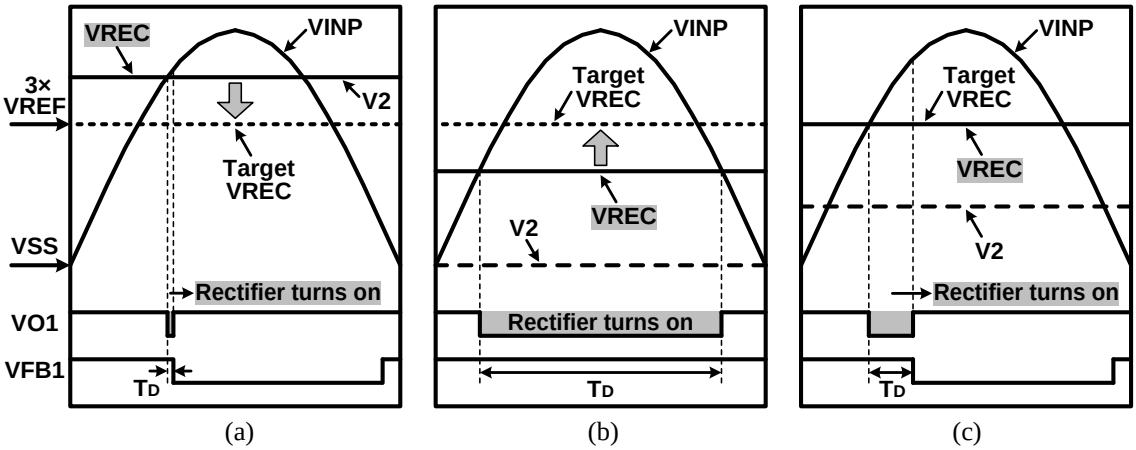


Fig. 6.6. Timing diagram of the adaptive rectifier when (a) $V_{REC} > 3V_{REF}$, (b) $V_{REC} < 3V_{REF}$, and (c) $V_{REC} = 3V_{REF}$.

In Fig. 6.5b, a startup circuit with R_1 and N_5 driven by V_{INN} guarantees the rectifier operation before V_{REC} is charged up without additional startup circuits used in chapter 3.3, and without affecting the normal rectifier operation after startup. The reset control circuit on the lower right resets the phase control feedback loop to turn off P_3 and P_6 after P_1 turns off and V_{INP} goes low. Here, the timing of the reset signal depends on V_{INP}, which unlike the process-dependent inverter delay in chapter 3.3, is independent of process variations.

6.4. Wireless Stimulating System with Adaptive Supply Control

6.4.1. Current Stimulator with Adaptive Supply Control

Each current driver has been equipped with a pair of 5-bit current sources with low dropout voltages, while being supplied from the adaptive V_{REC}, as shown in Fig. 6.7. Feedback loops using $AMP_{2\text{-}5}$ set the drain-source voltages of P_{14} ~ P_{18} and N_{15} ~ N_{19} at ~60 mV in the triode region. Therefore, the voltage headroom of the output stage, V_{Head}, can drop down to $V_{DS,sat}$ + 60 mV, which is smaller than $2V_{DS,sat}$ of a typical cascode output stage. The two current drivers source and sink at the same time through a pair of 4:1 site selectors, providing a bipolar stimulation compliance voltage of V_{REC} - $2V_{Head}$. The 5-bit current sources with binary-weighted transistors are placed at the output stage directly to reduce the stimulator power loss compared to using current mirrors after a 5-bit current DAC in [59].

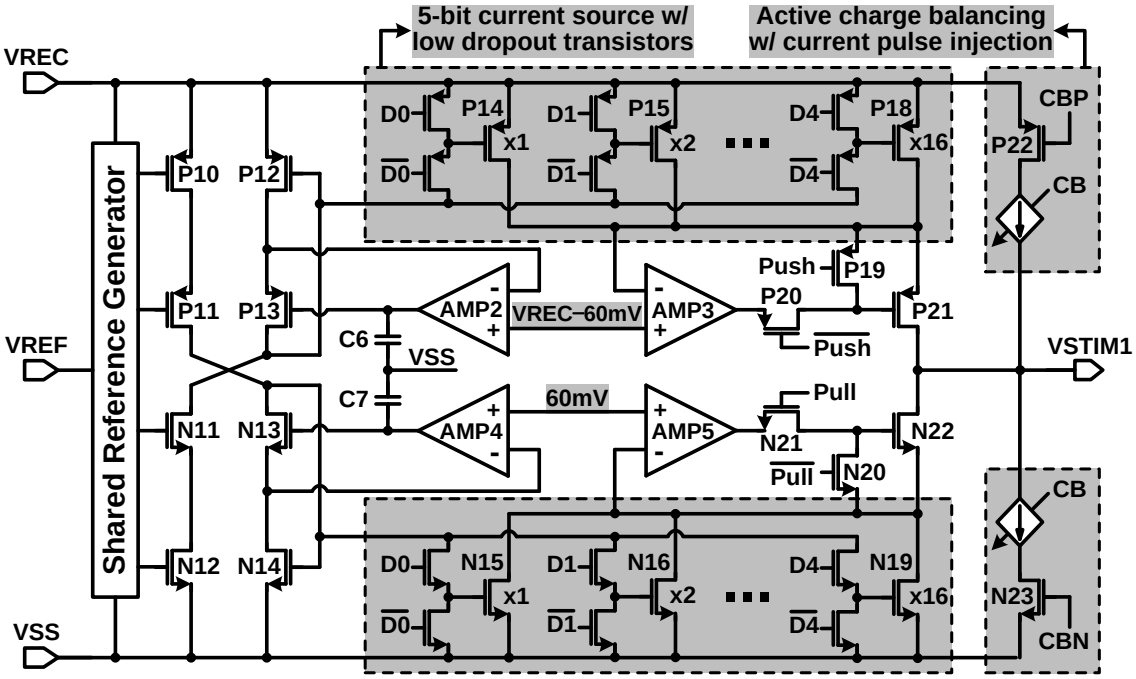


Fig. 6.7. Schematic diagram of the proposed current driver with low dropout 5-bit current sources and the active charge balancing.

Active charge balancing circuits push or pull additional small current pulses to the load after stimulation until the residual site voltage settles within a ±50 mV safety window [3]. To prevent the accumulation of unrecoverable charge in the tissue and utilize the residual voltage as a reliable indicator of charge imbalance, the electrode potential needs to be kept within a safe potential window during stimulation as well. This is known as the water window, where irreversible Faradaic reactions do not occur [49]. The active charge balancing scheme, utilized here, is capable of providing the small balancing current pulses and also estimating the required balancing period. Passive charge balancing schemes which short electrodes after stimulation, on the other hand, have difficulty defining the current and period needed for charge balancing [79].

In order to verify how the adaptive supply voltage, V_{REC}, in Fig. 6.7 increases the stimulation power efficiency compared to using the fixed supply voltage, V_{DD}, we analyzed the efficiency for both cases in Fig. 6.8.

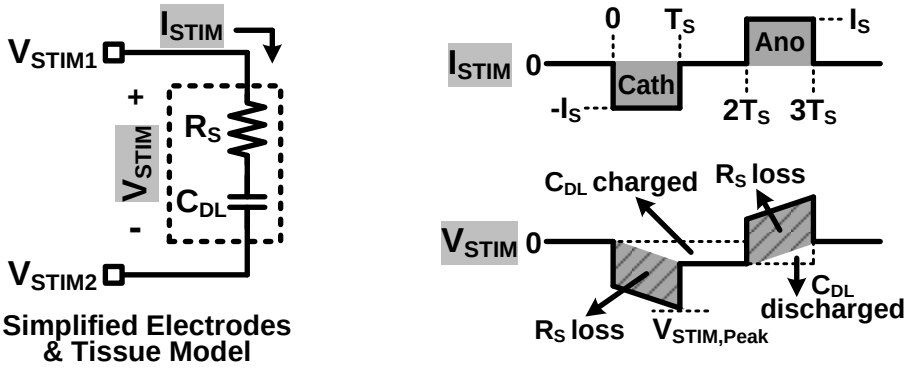


Fig. 6.8. Stimulation efficiency analysis using (a) a simplified electrodes and tissue model (R_S and C_{DL}), and (b) stimulation current and voltage waveforms.

In Fig. 6.8a, the electrodes and tissue model is simplified to a series R_S and C_{DL}, which represent the solution spreading resistance and the double-layer capacitance, respectively, while two current drivers across the two sites apply bipolar stimulation [79], [80]. Fig. 6.8b shows the stimulation current, I_{STIM}, and voltage, V_{STIM}, during the biphasic-bipolar stimulation with current amplitude, I_S, and pulse width, T_S. The power

transferred to the load during cathodic and anodic stimulations can be expressed as the R_S power loss plus the power charging or discharging C_{DL} by simply multiplying the instantaneous I_{STIM} and V_{STIM},

$$P_{Load(cath)} = \frac{1}{T_S}\int_0^{T_S} -I_S\left(-I_S R_S - \frac{1}{C_{DL}} I_S t\right) dt = {I_S}^2 R_S + \frac{1}{2C_{DL}} {I_S}^2 T_S \tag{6.1}$$

$$P_{Load(ano)} = \frac{1}{T_S}\int_{2T_S}^{3T_S} I_S \begin{pmatrix} -\frac{1}{C_{DL}} I_S T_S + I_S R_S \\ +\frac{1}{C_{DL}} I_S (t - 2T_S) \end{pmatrix} dt = {I_S}^2 R_S - \frac{1}{2C_{DL}} {I_S}^2 T_S \tag{6.2}$$

Negatively charged C_{DL} after cathodic phase decreases V_{STIM}, and results in smaller power delivered to the load during the anodic phase. The stimulation power efficiency with the fixed supply voltage, V_{DD}, can be defined as the ratio between the power transferred to the load and the power drained from the supply rails,

$$\eta_{STIM(Fixed)} = \frac{P_{Load(cath+ano)}}{P_{Supply}} = \frac{2{I_S}^2 R_S}{2(I_S + I_{Static})V_{DD}} \approx \frac{I_S R_S}{V_{DD}}, \quad if\ I_{Static} \ll I_S \tag{6.3}$$

where I_{Static} is the static current of the stimulator internal circuitry, which is ~14 μA in our design, and usually much smaller than the stimulation current.

In the proposed current stimulator, the adaptive supply voltage, V_{REC}, can be automatically adjusted as,

$$V_{REC} = \left|V_{STIM,Peak}\right| + 2V_{Head} = \left|V_{RS} + V_{CDL,peak}\right| + 2V_{Head} < V_{DD} \tag{6.4}$$

where $V_{STIM,peak}$ and $V_{CDL,peak}$ are the peak voltages across the electrode-tissue model and the C_{DL}, respectively, and V_{RS} is the voltage drop across R_S. By replacing V_{DD} in (6.3) with V_{REC} in (6.4), the stimulation power efficiency with the adaptive supply control can be expressed as,

$$\eta_{STIM(Adap)} = \frac{I_S R_S}{V_{REC}} = \frac{I_S R_S}{\left|V_{RS} + V_{CDL,peak}\right| + 2V_{Head}} = \frac{1}{1 + \frac{T_S}{R_S C_{DL}} + \frac{2V_{Head}}{I_S R_S}} \tag{6.5}$$

which is indeed higher than $\eta_{STIM(Fixed)}$ in (6.3).

$\eta_{STIM(Adap)}$ in (5) can be further simplified as,

$$\eta_{STIM(Adap)} \approx \frac{1}{1+\frac{T_S}{R_S C_{DL}}}, \quad if \;\; 2V_{Head} \ll V_{RS} \tag{6.6}$$

If V_{RS} >> V_{Head} (~150 mV in our design), $\eta_{STIM(Adap)}$ simplifies to a function of the electrode-tissue model parameters, R_S and C_{DL}, and stimulus pulse width, T_S. Large R_S results in more power transferred to the load, while large C_{DL} or small T_S decrease the required V_{REC}, leading to higher stimulation efficiency.

6.4.2. Voltage Readout Channel and Forward/Back Telemetry

Fig. 6.9 shows the schematic diagram of the voltage readout channel including a capacitive attenuator and a voltage detector. V_{STIM1} and V_{STIM2}, from the active sites, which can be as high as 4.6 V depending on the V_{REC}, are capacitively attenuated by $C_8/(C_8+C_9)$ during stimulation and charge balancing periods when EN = 1. After the charge balancing period, the capacitive attenuators are deactivated by disconnecting them from $V_{STIM1,2}$ (EN = 0) and then discharging C_8 and C_9 (EN_B = 1) to attenuate $V_{STIM1,2}$ accurately in the next stimulation period. The attenuated stimulation voltages, V_{S1} and V_{S2}, are applied to the voltage detector, which consists of a fixed-gain differential amplifier followed by a buffer, supplied at V_{DIG} = 1.8 V. As a result, the differential input signals are converted to a single-ended output voltage, V_{DET}, with a gain of R_3 / $2R_2$, which is then provided to the MCU to close the loop on adaptive supply control and application of the active charge balancing function.

The proposed wireless stimulating system is capable of communicating with forward and back data telemetry through the inductive link. Fig. 6.10 shows the schematic diagrams of the clock and data recovery circuits, which are used for setting the stimulation parameters and active channels through the MCU. The clock recovery in Fig. 6.10a adopts the latch comparator with cross-coupled P_{23} and P_{24} followed by inverters to generate the clock signal from the power carrier, $V_{INP,N}$, with low power consumption.

The data recovery consists of an envelope detector and an amplitude shift keying (ASK) demodulator, as shown in Fig. 6.10b and 6.10c, respectively.

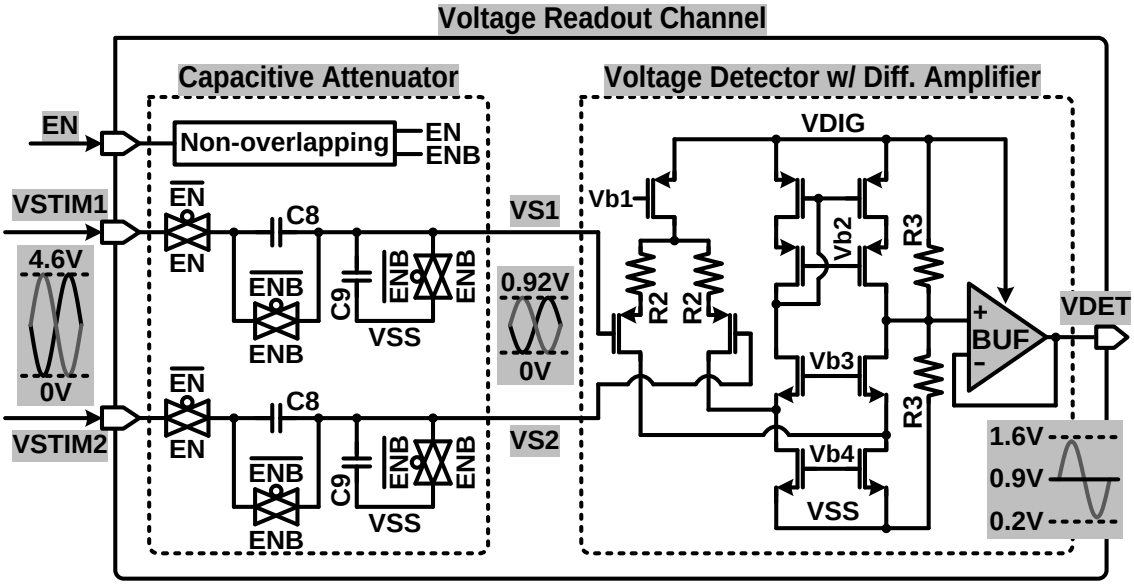


Fig. 6.9. Schematic diagram of the voltage readout channel including the capacitive attenuator and voltage detector, which are used for both adaptive supply control and active charge balancing.

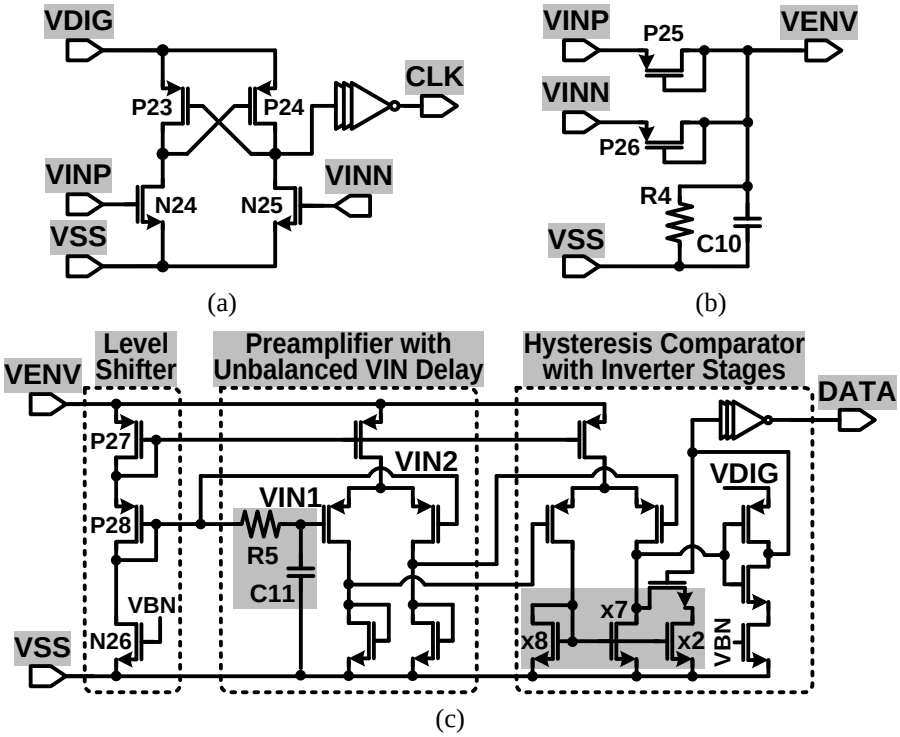


Fig. 6.10. Schematic diagrams of (a) the clock recovery, (b) the envelope detector, and (c) the ASK demodulator for the forward data telemetry.

In Fig. 6.10b, the diode-connected passive rectifiers, P_{25} and P_{26}, extract the envelope voltage, V_{ENV}, from the amplitude shift keyed power carrier, $V_{INP,N}$. V_{ENV} is applied to the demodulator in Fig. 6.10c, which includes a level shifter, a preamplifier, and a hysteresis comparator, to recover the data signal. The level shifter provides bias voltage to the rest of the circuit through P_{27}, while shifting V_{ENV} down through P_{27}-P_{28} to the preamplifier input range. The preamplifier has unbalanced delays, via R_5 and C_{11}, at its inputs, V_{IN1} and V_{IN2}, to detect and amplify the amplitude variations of V_{ENV}. Finally, the hysteresis comparator, which utilizes the size mismatch of its current mirror, converts the preamplifier outputs to the recovered serial data bit stream at V_{DIG} level through several inverters. The serial data is then oversampled by the clock signal in the MCU and saved in its registers. The back telemetry link utilizes the SC switches across *L2*, N_3 and N_4 in Fig. 6.5a, to provide LSK modulation [9].

6.5. Measurement Results

The inductively powered wireless stimulating system was fabricated in the ON-Semiconductor 0.5-µm 3M2P n-well standard CMOS process. Fig. 6.11 shows a chip micrograph and floor plan of the proposed wireless adaptive stimulating system, occupying 2.25 mm^2 including pads.

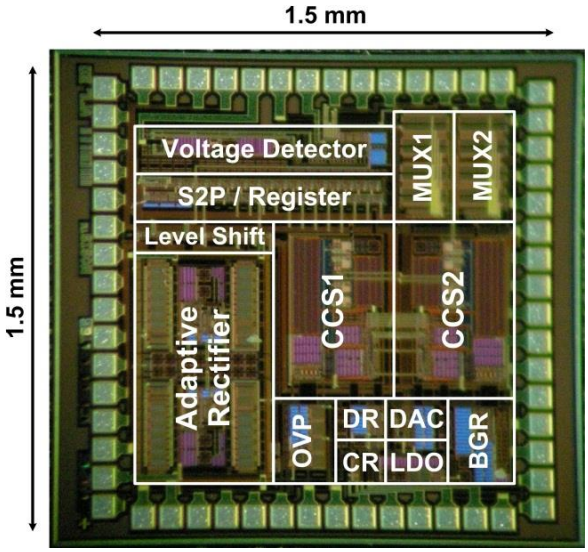


Fig. 6.11. Chip micrograph of the wireless stimulating system.

In our test setup, a class-E power amplifier drives the inductive link, which specifications are shown in Table 6.1, to provide the wireless stimulating system with a 2 MHz sinusoidal input. The off-chip MCU (MSP430) from Texas Instruments (Dallas, TX) was chosen for its versatility and ultra-low power consumption [81].

Table 6.1: *In Vitro* Test Setup Specifications

Power transmitter	Class-E PA
Carrier frequency (f_C)	2 MHz
Primary coil diameter / inductance (L_1)	4.0 cm / 6.8 μH
Secondary coil diameter / inductance (L_2)	1.0 cm / 1.2 μH
Distance between L_1 and L_2	1.5 cm
Electrodes (4-channel)	Quartz-platinum/tungsten
Electrode length / diameter / tip	15 mm / 80 μm / 1 mm
Electrode spacing (pitch)	3 mm
Electrodes + saline impedance @ 2.5 kHz	3.8 kΩ + 80 nF in series

6.5.1. Adaptive Rectifier with Adjustable V_{REC}

Measured waveforms in Fig. 6.12 show how the adaptive rectifier controls its turn-on phase depending on the 3-bit phase control input, *CTL*, to adjust V_{REC} when $V_{INP,N}$ peak is constant at 5 V, load current is set to 2 mA, and f_C = 2 MHz. When *CTL* = 000 and V_{REF} = 0.83 V, the adaptive rectifier turns on within 50 ns of the beginning of the carrier cycle (θ = 36°), once $V_{INP,N} > V_{REC}$, and turns off after only 20 ns because the amount of delivered power is sufficient to increase V_{REC} to the desired level of 2.5 V. When *CTL* = 011 and V_{REF} = 1.13 V, the onset of rectifier turn-on shifts to 66 ns from the beginning of the carrier cycle (θ = 47.5°) and the on period adaptively increases to 28 ns to generate a higher V_{REC} = 3.4 V. When *CTL* = 111 and V_{REF} = 1.53 V, the adaptive rectifier operates almost like a regular active synchronous rectifier with θ = 68.4° and the on-time of 65 ns until $V_{INP,N}$ goes below V_{REC}, while delivering more power to achieve the highest possible V_{REC} = 4.6 V. In addition, when V_{REC} = 2.5 V with I_{OUT} = 2 mA, the adaptive rectifier results in a small $\Delta V_{REC} < 3$ mV against $V_{IN,peak}$ variations within 3 V to

5 V. This rapid line regulation capability is an additional benefit of the phase control feedback mechanism.

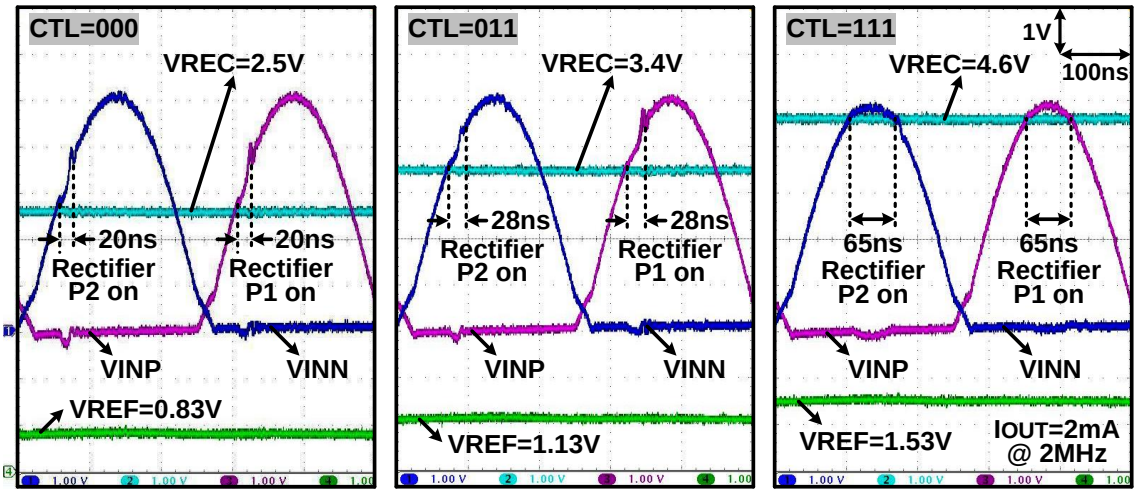


Fig. 6.12. Measured waveforms of the adaptive rectifier generating the multilevel V_{REC} from 5 V peak constant $V_{INP,N}$ depending on the 3-bit *CTL* input. In each case, I_{OUT} is set at 2 mA and f_C = 2 MHz.

Fig. 6.13 shows the adaptive rectifier PCE vs. V_{REC} with $V_{INP,N}$ peak and load current kept constant at 5 V and 2.8 mA (the highest I_{STIM} = 2.48 mA for this stimulator), respectively.

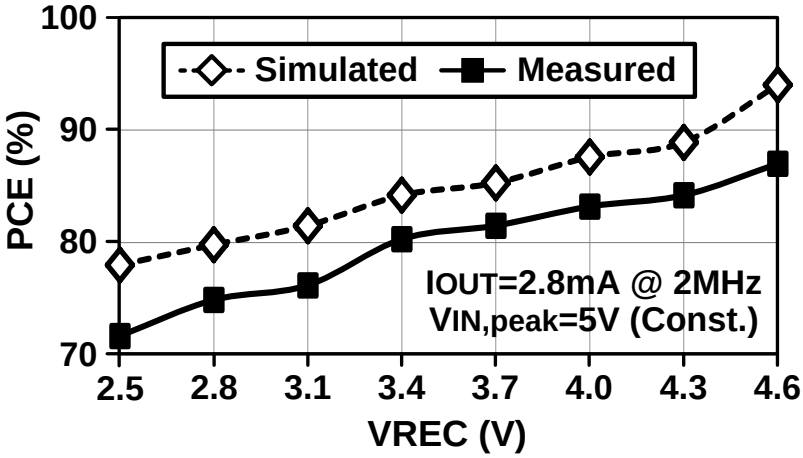


Fig. 6.13. Measured and simulated PCE vs. V_{REC} of the adaptive rectifier. Peak of V_{INP} = V_{INN} = 5 V, f_C = 2 MHz, and I_{OUT} = 2.8 mA.

The adaptive rectifier achieves competitive PCEs of 78 ~ 94% and 72 ~ 87% in simulation and measurement, respectively, while providing unique multilevel adaptive

V_{REC} output between 2.5 ~ 4.6 V, controlled by its 3-bit input. The PCE slightly decreases with lower V_{REC} because the rectifier dropout voltage becomes a larger percentage of V_{REC}, and the on-resistance of the rectifying switches increase at lower voltages. Nonetheless, the adaptive rectifier still achieves considerably higher PCE than using a conventional rectifier followed by an adjustable regulator to generate the desired DC voltage. The difference between simulated and measured PCEs may be the result of mismatches between rectifying switches and their phase control comparators, as well as the effects of parasitic inductance and capacitance of the measurement setup, as explained in chapter 2.2.5.

6.5.2. Adaptive Supply Control and Active Charge Balancing

Measured waveforms of the stimulator outputs, $V_{STIM1,2}$, and the voltage detector output, V_{DET}, are shown in Fig. 6.14 when ±1.04 mA biphasic-bipolar stimulus currents at T_S = 400 μs flow between $V_{STIM1,2}$ through a series R_SC_{DL} load, which was chosen to be 2 kΩ and 500 nF for the DBS application [58], [82]. For closed-loop adaptive supply control, the MCU samples V_{DET} at the end of the cathodic phase to measure $V_{STIM,peak}$ in Fig. 6.8. The adaptive rectifier receives the phase control signals and automatically adjusts V_{REC} to be 0.2 ~ 0.5 V higher than $V_{STIM,peak}$, to keep a small voltage drop across the stimulating current source, ΔV, for high stimulation efficiency. The MCU samples V_{DET} again at the end of stimulation (anodic phase) to check the residual voltage between electrodes. If the voltage falls outside a safe window, set to ±50 mV, the active charge balancing circuit injects either a small positive or a negative current pulse (adjustable ±20 μA for 20 μs), and repeats the sampling procedure via the MCU until the residual charge is neutralized.

Fig. 6.15 compares the stimulator supply voltage and PCE vs. I_{STIM} graphs between adaptive, V_{REC}, and fixed, V_{DD}, supplies when R_S = 2 kΩ, C_{DL} = 500 nF, and T_S = 400 μs. In Fig. 6.15a, the adaptive V_{REC} was measured with 0.3 V increments between 2.5

V and 4.6 V vs. I_{STIM}. In these measurements, V_{REC} - $V_{STIM,peak}$ < 0.2 V, while the fixed V_{DD} was measured at 4.6 V. Fig 6.15b compares the stimulation power efficiencies vs. I_{STIM} between the fixed and adaptive mechanisms, using the measured supply voltages in Fig. 6.15a as well as (6.3) and (6.5), respectively, while including the stimulator I_{Static} = 14 μA.

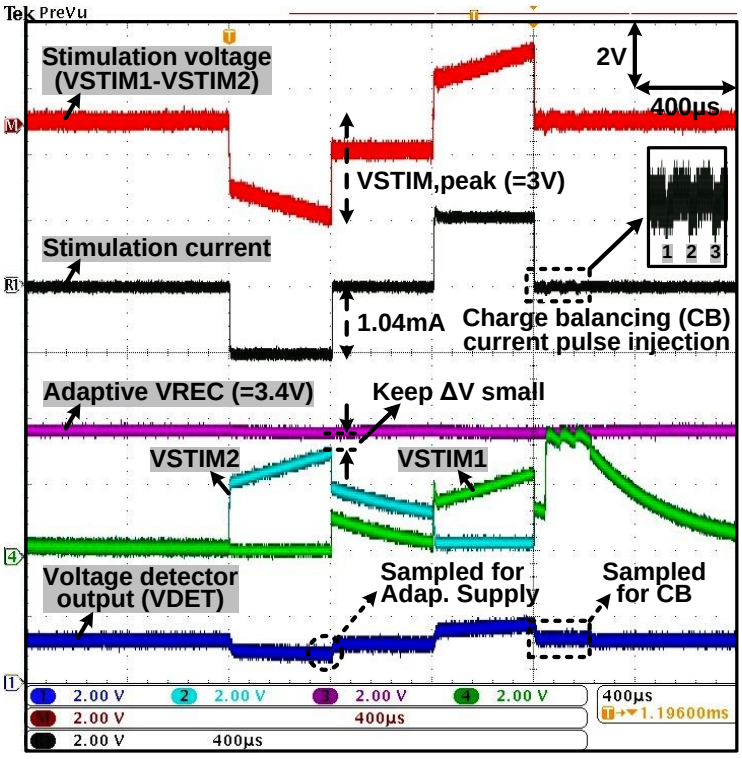
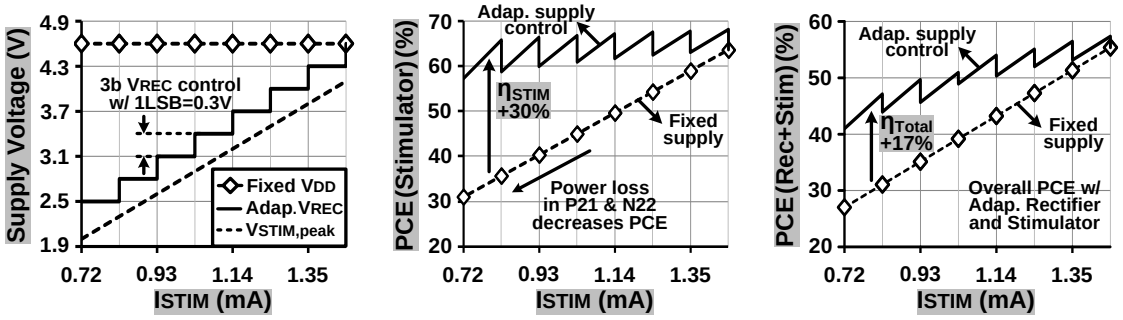


Fig. 6.14. Measured waveforms of the current stimulator with R_S = 2 kΩ and C_{DL} = 500 nF connected in series between two active sites, as shown in Fig. 6.7, demonstrating the adaptive V_{REC} control and active charge balancing operations through the voltage readout channel.



(a) (b) (c)

Fig. 6.15. (a) Adaptive V_{REC} and fixed V_{DD} vs. I_{STIM}, (b) stimulation power efficiencies vs. I_{STIM}, and (c) overall power efficiencies, *i.e.* rectifier + stimulator, vs. I_{STIM}. Solid line: adaptive supply control, dashed line: fixed supply, electrode-tissue model: R_S = 2 kΩ and C_{DL} = 500 nF in series, and T_S = 400 μs.

As expected, with lower I_{STIM}, the large voltage difference between V_{DD} and V_{STIM} increases the power loss in the stimulator output stage (P_{21} and N_{22} in Fig. 6.7), degrading the fixed voltage stimulation power efficiency. On the other hand, the adaptive V_{REC} keeps the voltage difference across the stimulator output small to minimize the power loss regardless of the I_{STIM} variations. As a result, the stimulation power efficiency with the adaptive supply control (58 ~ 68%) is up to 30% higher than the fixed V_{DD} (31 ~ 63%). In Fig. 6.15c, the overall power efficiencies from secondary coil, L_2, to the load were calculated by multiplying the measured PCE of the adaptive rectifier in Fig. 6.13 and the stimulation efficiency in Fig. 6.15b. Since the adaptive rectifier achieves relatively high PCEs even with lower V_{REC} levels, adaptive supply control still leads to higher overall power efficiencies (41 ~ 58%) compared with using a fixed supply (27 ~ 55%).

The MCU consumes ~19 μA in the standby mode and ~400 μA for running the ADC and generating control signals at V_{DIG} = 1.8 V and *CLK* = 2 MHz. Power consumption for these functions can be significantly reduced by sampling the peak stimulation voltage periodically, *e.g.* once every 10 ~ 20 cycles, to occasionally adjust the *CTL*. Moreover, the MCU functions can be integrated on chip by a low-power 3-bit SAR-ADC for generating the 3-bit *CTL* signal and simple control logic, leading to much lower power consumption compared to the off-chip MCU in the current prototype.

INL and DNL of the 5-bit cathodic/anodic stimulus currents, I_{STIM1} and I_{STIM2}, for bipolar stimulation were measured and presented in Fig. 6.16 along with the stimulation current mismatch, $\Delta I_{STIM} = I_{STIM1} - I_{STIM2}$. Both I_{STIM1} and I_{STIM2} show similar tendencies between 0.08 mA and 2.48 mA with 5-bit resolution, achieving the maximum INL and DNL of 0.43 and 0.17 LSB, respectively. The maximum ΔI_{STIM} between I_{STIM1} and I_{STIM2} was ~4 μA.

Fig. 6.17 shows the measured waveforms of the clock recovery and the ASK-demodulated data recovery blocks for the forward data telemetry. In Fig. 6.17a, a 2 MHz

clock signal, *CLK*, has been recovered from the 2 MHz carrier signal. In Fig. 6.17b, the amplitude variations of the primary coil voltage at 5.8% (= 3.8 V / 65.2 V) modulation index, induced across *L2*, have resulted in ~100 mV variations in V_{ENV}. The ASK demodulator has then recovered the serial data bit stream, *DATA*, at 50 kbps.

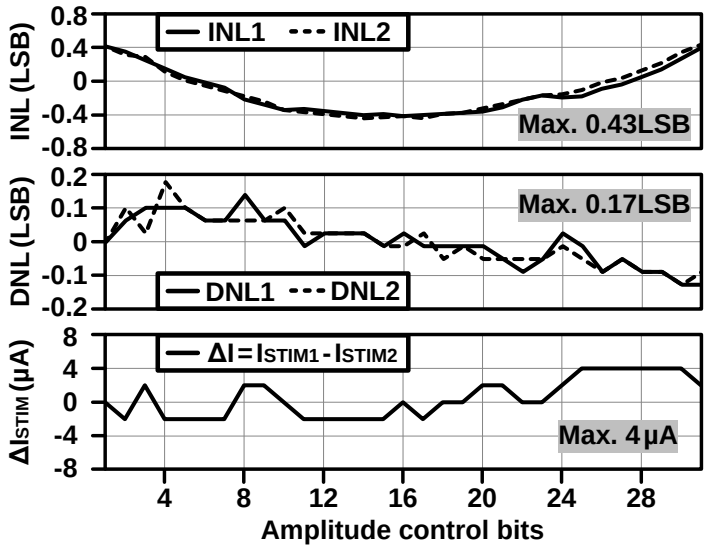
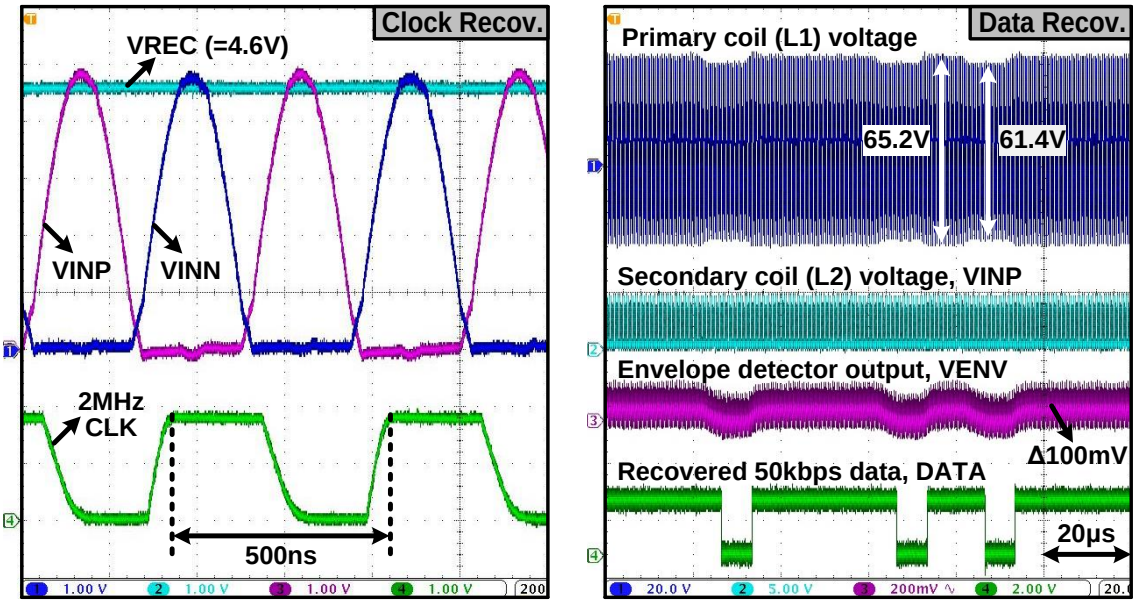


Fig. 6.16. Measured INL and DNL of the 5-bit I_{STIM1} for cathodic stimulation and I_{STIM2} for anodic stimulation along with the stimulation current mismatch, ΔI_{STIM}, between I_{STIM1} and I_{STIM2}.



(a) (b)

Fig. 6.17. Measured waveforms of (a) the 2 MHz clock recovery, and (b) 50 kbps data recovery from the 2 MHz power carrier at 5.8% ASK modulation index.

6.5.3. *In Vitro* Experiments

The proposed wireless stimulating system was verified through *in vitro* experiments using quartz-platinum/tungsten electrodes (EF8025, Thomas Recording, Giessen, Germany) and saline solution, as shown in Fig. 6.18. To emulate the DBS stimulation, 4 electrodes were aligned in parallel with 3 mm pitch spacing and soaked in 0.9% NaCl solution, which represents the brain tissue conductivity [83], [84]. The measured average impedance between adjacent electrodes in the solution was ~3.8 kΩ and 80 nF in series at 2.5 kHz. Table 6.1 summarizes the *in vitro* test setup specifications.

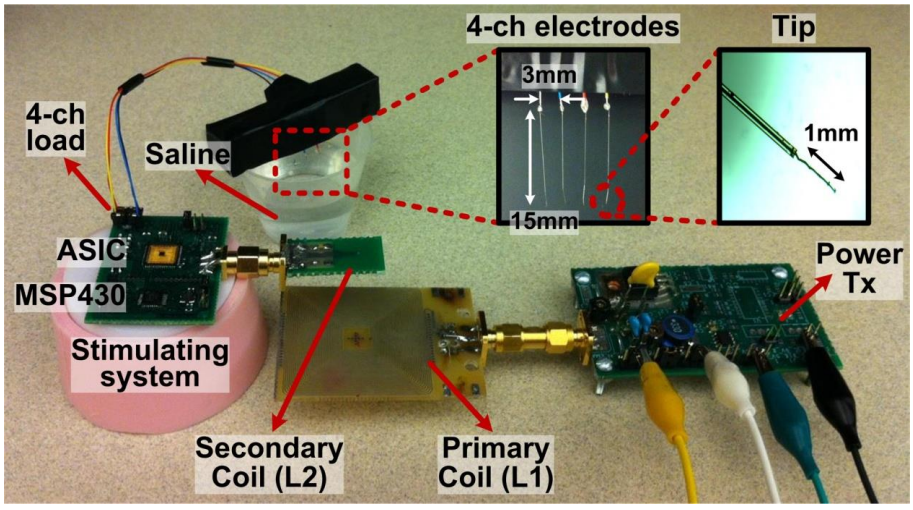


Fig. 6.18. Test setup for *in vitro* experiments using the wireless adaptive stimulator including an inductive link operating at 2 MHz and 4 platinum/ tungsten electrodes soaked in saline solution to emulate the DBS application.

Fig. 6.19 shows the measured stimulation waveforms from the *in vitro* experiments, focusing on the stimulator's adaptive supply control, active charge balancing, and multi-channel stimulation capabilities. In Fig. 6.19a, two different stimulation currents, ±240 μA and ±480 μA, were applied to the saline solution through electrodes, and the supply voltage, V_{REC}, was automatically set to 2.8 V and 3.4 V, respectively, which maximize the stimulation efficiency. At the same time, the active charge balancing mechanism ensured that the residual charge was neutralized following biphasic stimulation. Fig. 6.19b shows the multi-channel stimulation waveforms among 4

electrodes. The selected channels sourced and sinked ±560 µA and 400 µs stimulus pulses at 250 Hz, while the other channels were floating.

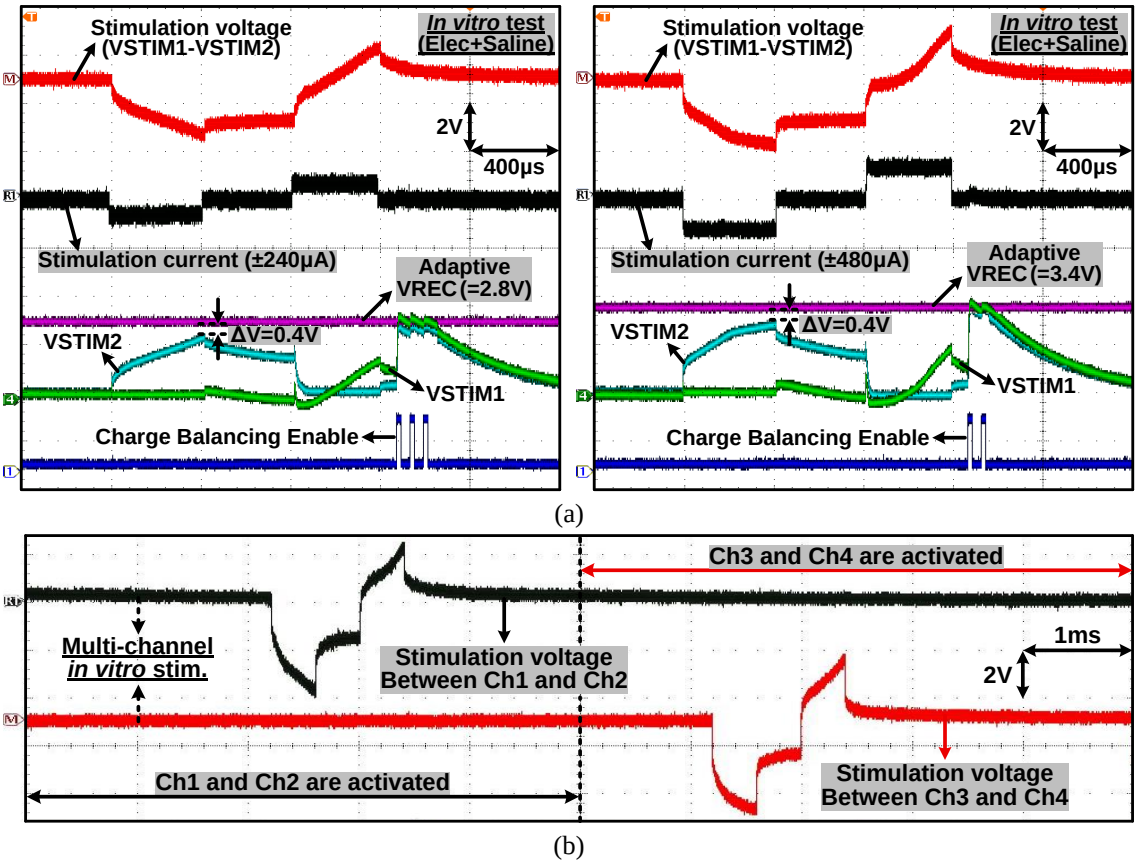


Fig. 6.19. Measured stimulation waveforms from the *in vitro* experiments showing (a) adaptive supply control with different stimulation currents, active charge balancing, and (b) multi-channel stimulation capability.

6.5.4. Performance Summary and Discussion

Table 6.2 benchmarks the proposed adaptive rectifier that was presented in chapter 6.3 against several recently published active rectifiers. While being capable of generating multilevel output voltages between 2.5 V and 4.6 V from a constant 5V peak AC input, the adaptive rectifier maintains high measured PCE of 72 ~ 87%, depending on the V_{REC} level, when delivering 2.8 mA to the load. The voltage conversion efficiency, VCE (= V_{REC} / $V_{IN,peak}$), reaches as high as 92% when V_{REC} = 4.6 V.

Table 6.2: Adaptive Rectifier Benchmarking

Publication		2008 [30]	2009 [32]	2009 [31]	2012 [67]	**This work**
Technology		0.5µm	0.18µm	0.35µm	0.18µm	**0.5µm CMOS**
AC-DC Structure		Active Rec.	Active Rec.	Active Rec.	Active Rec.	**Adaptive Output Active Rectifier**
$V_{IN,\,peak}$ (V)		5	1.25	2.4	1.5	**5**
V_{REC} (V)		4.36	0.96	2.08	1.33	**2.5 ~ 4.6 (3-bit)**
VCE (%)		87.2	76.8	86.7	89	**50 ~ 92**
R_L (kΩ)		1	2	0.1	1	**I_L = 2.8 mA**
f_C (MHz)		1	10	1.5	13.56	**2**
Area (mm^2)		0.4	0.86	0.4	0.009	**0.3**
PCE (%)	Sim.	90.4	N/A	87	N/A	**78 ~ 94**
	Meas.	84.8	76	N/A	81.9	**72 ~ 87**

Table 6.3 summarizes the overall specifications of the proposed wireless stimulating system. The current stimulator achieves 58 ~ 68% power efficiency regardless of the I_{STIM} and V_{STIM} variations thanks to the adaptive supply control mechanism. It should be noted that the stimulation efficiency may also vary depending on the electrode/tissue impedance and the stimulus pulse width, as shown in (6.6).

Table 6.3: Wireless Stimulating System Specifications

Overall System		**Current Stimulator**	
Process	0.5 µm CMOS	# output ch.	4-ch (DBS)
ASIC area	2.25 mm^2	Stim. rate	15.6 ~ 500 Hz*
Power source	Inductive link	Pulse width	16 ~ 512 µs*
Power Management		Current range	0.08~2.48mA (5b)
Adjustable V_{REC}	2.5 ~ 4.6V (3b)	INL / DNL	0.43 / 0.17 LSB
Measured PCE	72 ~ 87%	Ch. max. ΔI	4 µA
V_{DIG}	1.8 V	I_{Static}	14 µA**
OVP threshold	$V_{IN,peak}$ > 5.8V	V_{Head}	150 mV
Back telemetry	short-coil LSK	Charge balan.	Active pulse injection
Forward Telemetry		Stim. PCE	58 ~ 68%***
Clock freq.	2 MHz	**Voltage Readout Channel**	
ASK data rate	50 kbps	In/out range	0~4.6 V / 0.2~1.6 V
Modul. index	5.8%	I_{Static}	12 µA**

* Adjustable in MCU, ** Simulation, *** Vary with load model and pulse width

In the case of stimulating through multiple electrodes with different peak voltages, the adaptive supply voltage needs to follow the highest site voltage to properly stimulate

all sites, limiting the improvement achieved in stimulation efficiency. This is why we recommend this technique for applications, such as DBS, which involve a relatively small number of macro sites that have similar properties. In applications with a large number of sites, such as retinal implants, it is conceivable to divide the sites into smaller subsets and use multiple independent adaptive rectifiers and current drivers, one per subset, at the cost of larger chip area.

The proposed system dissipates a maximum power of ~15 mW, assuming constantly flowing stimulus current, resulting in temperature rise well below the safe 1 °C limit [85]. If the efficiency of the transcutaneous inductive link is 60% at 10 mm coil separation from [17], the necessary Tx power at 2 MHz can be estimated at ~25 mW. This is well below the FCC's 100 mW/cm^2 limit for maximum permissible exposure (MPE) within 0.3 ~ 3 MHz [86].

CHAPTER VII

A POWER-EFFICIENT SWITCHED-CAPACITOR STIMULATING (SCS) SYSTEM FOR ELECTRICAL AND OPTICAL STIMULATION

7.1. Introduction

Deep brain stimulation (DBS) has been proven as an effective therapy to alleviate Parkinson's disease, tremor, and dystonia [48], [49]. Traditional DBS devices have used large primary batteries implanted in the chest area, which need to be replaced every 2~5 years through surgery [50]. Moreover, subcutaneous interconnects from batteries pass across the neck to reach the electrodes implanted deep in the brain, resulting in risk of mechanical failure due to head motion. Towards less invasive head-mounted DBS, we have utilized an inductive transcutaneous link from a behind the ear (BTE) rechargeable energy source, similar to cochlear implants, to provide sufficient power without size, lifetime, and discomfort of chest-mounted battery-powered traditional DBS [1].

The next step is adopting aggressive power management schemes to further improve the DBS efficiency. Voltage-controlled stimulation (VCS) enables power-efficient stimulation, while balancing the stimulation charge is quite complicated in VCS because the electrode impedance varies over time and position [52], [53]. On the contrary, current-controlled stimulation (CCS) provides precise charge control and safe operation, but it has low power efficiency due to the dropout voltage across current sources [47], [58]. Switched-capacitor stimulation (SCS), proposed in [87], takes advantage of both high efficiency and safety using capacitor banks to transfer charge to the tissue, but it requires an efficient on-chip capacitor charging system, directly from the inductive link. Here, we present the first integrated wireless SCS system-on-a-chip with inductive capacitor charging and charge-based stimulation capabilities, which can improve both stimulator (before electrodes) and stimulus (after electrodes) efficiencies in DBS.

Fig. 7.1 compares the conventional CCS with the proposed SCS while emphasizing the inductive power flow and stimulus waveform shapes. The CCS requires

a rectifier, a regulator, and an array of current sources to generate a rectangular stimulus. Power losses at each stage result in poor overall stimulator efficiency, which is defined as the stimulator output power over input power from the L_2C_2 tank. On the contrary, the inductively powered SCS efficiently charges the storage capacitors directly from the inductive link and delivers the stored charge to the tissue (series *RC*), improving stimulator efficiency. In addition, the proposed SCS is capable of generating a decaying-exponential stimulus by dumping charge in capacitors to the tissue without wasting additional power. The decaying-exponential stimulus can be more effective in activating the target tissue than conventional rectangular or ramp stimulus when consuming the same amount of energy, improving both stimulus efficiency and safety [61], [62].

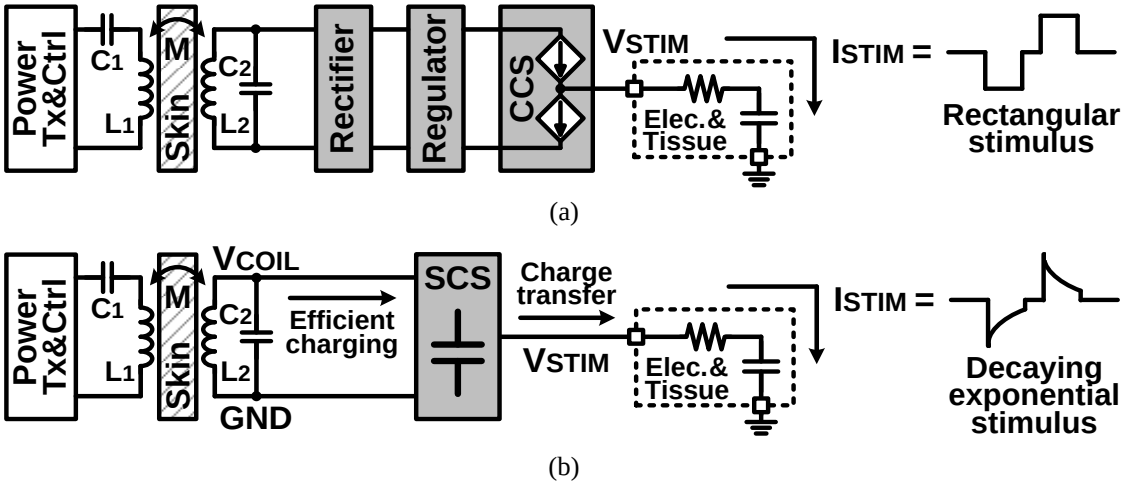


Fig. 7.1. Conceptual diagrams of (a) the conventional CCS and (b) the proposed SCS.

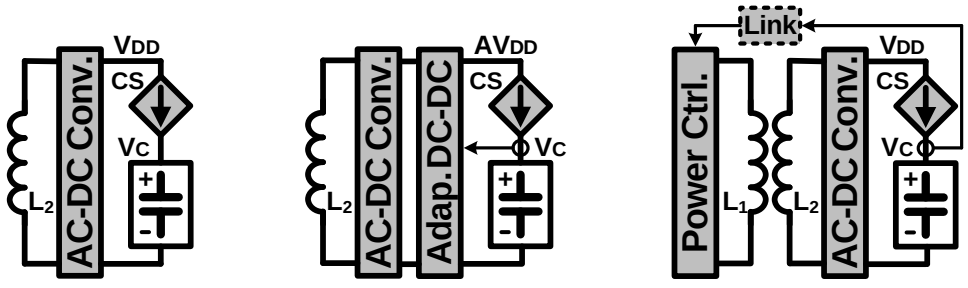
Moreover, direct optical stimulation of neural cells, called optogenetics, has become another effective way to activate genetically modified neurons by using various light-delivery schemes with LEDs because of its fast, spatially controlled, and minimally invasive modulation of cellular activity [88], [89]. However, LEDs typically require high instantaneous power to emit sufficient light for optical stimulation, which is a limiting factor in conventional inductively powered devices because the load variation affects the coil coupling, degrading the inductive power transmission [90]. To address this limitation,

we have also utilized the SCS system for power-efficient optogenetics by periodically discharging the capacitors into LEDs, providing high instantaneous current to LED arrays.

7.2. A Wireless Capacitor Charging System through Inductive Links

7.1.1. Capacitor Charging Concept

Charging capacitors from a voltage source through a switch achieves maximum 50% efficiency, wasting half of input energy in the switch. On the other hand, charging capacitors with a current source can minimize the switching loss as the fixed charging current becomes smaller [91]. Fig. 7.2 shows the conventional Li-ion battery charging techniques in inductively powered devices. AC-DC converters, *e.g.* a rectifier or a voltage doubler, convert an AC input voltage from an inductive link to a DC supply voltage, V_{DD}, resulting in AC-DC power loss. In Fig. 7.2a, the current source charges the capacitor directly without switches by controlling its gate voltage [92]. However, the current source still wastes energy because of the difference between supply and capacitor voltages, V_{DD} - V_C. Generating an adaptive supply voltage, AV_{DD}, in Fig. 7.2b keeps the dropout voltage of the current source small, AV_{DD} - V_C, while suffering from the additional DC-DC power loss [93]. The charging system in Fig. 7.2c utilizes a back telemetry link to control the inductive power, adjusting V_{DD} depending on the V_C level to reduce the voltage drop across the current source [94]. However, it requires additional sensing and control circuits as well as an external feedback loop through an optical link.



(a) (b) (c)

Fig. 7.2. Conventional inductive Li-ion battery charging techniques in current source (CS) mode from (a) a fixed supply voltage [92], (b) an adaptive supply voltage [93], and (c) a supply voltage adjusted by an external control loop [94].

The concept of the proposed capacitor charging system starts from utilizing a series charge injection capacitor as a current source, which generates a fixed amount of predefined charging current. Fig. 7.3 shows the simplified circuit diagram of the inductive capacitor charging system, which charges a pair of positive and negative capacitors, C_P and C_N, respectively.

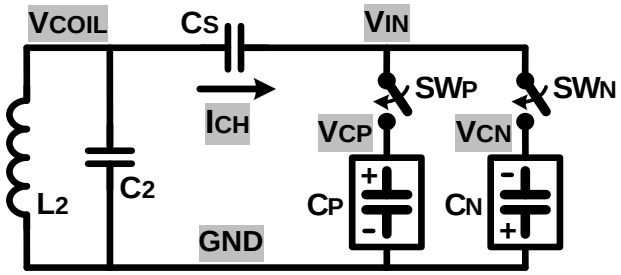


Fig. 7.3. Simplified circuit diagram of the inductive capacitor charging system.

The secondary coil, L_2, and its parallel resonant capacitor, C_2, which generate a coil voltage, V_{COIL}, are followed by a series charge injection capacitor, C_S, which provides an input voltage, V_{IN}, to C_P and C_N through switches, SW_P and SW_N, respectively. SW_P turns on when $V_{IN} > V_{CP}$ for positive C_P charging, and SW_N turns on when $V_{IN} < V_{CN}$ for negative C_N charging with respect to the ground, *GND*. When $V_{CN} < V_{IN} < V_{CP}$, both switches turn off, and V_{IN} follows V_{COIL}. Then, when either SW_P or SW_N turns on, the switch connects V_{IN} to a positive or negative capacitor voltage, V_{CP} or V_{CN}, holding V_{IN} relatively constant and generating a fixed charging current, I_{CH}, through C_S. For example, when $V_{IN} > V_{CP}$, SW_P connects V_{IN} to V_{CP} to hold V_{IN} around V_{CP}, while V_{COIL} keeps increasing. Thus, the voltage variation across C_S, V_{COIL} - V_{IN}, generates the positive I_{CH} until V_{COIL} reaches its positive peak. When V_{COIL} starts decreasing from its peak, V_{IN} also decreases below V_{CP}, and SW_P turns off. The charging current, I_{CH}, can be expressed as,

$$I_{CH} = C_S \times d(V_{COIL} - V_{IN})/dt \tag{7.1}$$

The I_{CH} value can be adjusted by choosing proper C_S, which will be discussed in chapter 7.1.2. Fixed I_{CH} minimizes the switch loss, while unlike a real current source the

voltage drop across C_S does not dissipate power, improving the charging efficiency from L_2 to the capacitor pair.

7.1.2. Charging Time and Efficiency Analysis

The smaller the charging current, the higher the capacitor charging efficiency and the smaller the power loss in switches, leading to longer charging time. Hence, the charging current, I_{CH}, should be optimized to charge the capacitors efficiently within a desired period. We modeled the charging time and efficiency depending on I_{CH} with simplified voltage and current waveforms of the capacitor charging system in Fig. 7.4. In this analysis, f_c is the carrier frequency that is received via V_{COIL}, n is the number of charging cycle, and $t[n]$ is the transition time of V_{IN} when $V_{CN} < V_{IN} < V_{CP}$. In this simplified model, we assume: 1) V_{COIL} is sinusoidal with a constant peak voltage, V_{Peak}, 2) switches turn on and off at ideal times, and V_{IN} becomes equal to V_{CP} or V_{CN} with negligible voltage drop across closed switches when connected to capacitors, 3) during each charging cycle, V_{CP} and V_{CN} are constant, and small voltage increments, ΔV_{CP} and ΔV_{CN}, are added to V_{CP} and V_{CN} at the end of each cycle, respectively, and 4) C_P and C_N are equal and charged by the same amount of I_{CH}, *i.e.* $V_{CP} = -V_{CN}$.

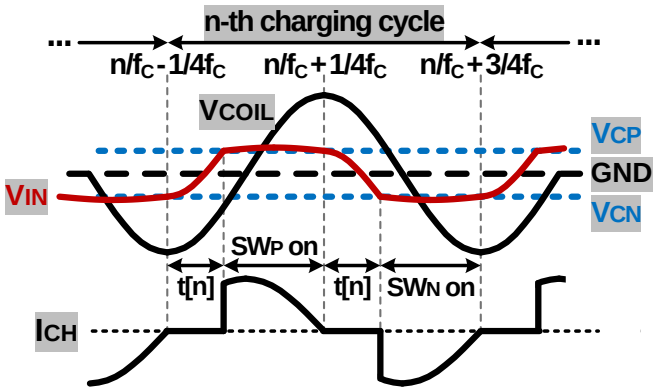


Fig. 7.4. Simplified voltage and current waveforms of the capacitor charging system for modeling and theoretical analysis.

When V_{IN} is connected to V_{CP} or V_{CN} for charging, V_{COIL} and I_{CH} can be expressed as,

$$V_{COIL}(t) = V_{Peak} sin(2\pi f_c t) \tag{7.2}$$

$$I_{CH}(t) = 2\pi f_c C_S V_{Peak} cos(2\pi f_c t) \tag{7.3}$$

V_{CP} at the n-th charging cycle, $V_{CP}[n]$, can be obtained from,

$$V_{CP}[n] = \sum_{i=1}^{n} \Delta V_{CP}[i] \tag{7.4}$$

where $\Delta V_{CP}[n]$ is the V_{CP} increment at the n-th charging cycle, from the initial condition of $V_{CP}[0] = V_{CN}[0] = 0$ V.

At the n-th charging cycle, $t[n]$ is equal to the transition time, in which V_{IN} increases from $V_{CN}[n\text{-}1]$ to $V_{CP}[n\text{-}1]$. Therefore,

$$V_{CP}[n-1] - V_{CN}[n-1] = 2V_{CP}[n-1]$$

$$= [V_{COIL}(t)]_{\frac{n}{f_c}-\frac{1}{4f_c}+t[n]}^{\frac{n}{f_c}+\frac{1}{4f_c}} = V_{Peak}[sin(2\pi f_c t)]_{\frac{n}{f_c}-\frac{1}{4f_c}+t[n]}^{\frac{n}{f_c}+\frac{1}{4f_c}} \tag{7.5}$$

In (7.5), $t[n]$ can be written as,

$$t[n] = \frac{sin^{-1}\left(-1 + \frac{2V_{CP}[n-1]}{V_{Peak}}\right)}{2\pi f_c} + \frac{1}{4f_c} \tag{7.6}$$

With $t[n]$ in (7.6), $\Delta V_{CP}[n]$ can be derived as,

$$\Delta V_{CP}[n] = \frac{1}{C_P}\int_{\frac{n}{f_c}-\frac{1}{4f_c}+t[n]}^{\frac{n}{f_c}+\frac{1}{4f_c}} I_{CH}(t)\,dt = \frac{C_S}{C_P} V_{Peak}[sin(2\pi f_c t)]_{\frac{n}{f_c}-\frac{1}{4f_c}+t[n]}^{\frac{n}{f_c}+\frac{1}{4f_c}}$$

$$= 2\frac{C_S}{C_P} V_{Peak}\left(1 - \frac{V_{CP}[n-1]}{V_{Peak}}\right) \tag{7.7}$$

Therefore, the charging period, T_{CH}, during which C_P and C_N are charged to a target charging voltage, $\pm V_{TG}$, at the n_{CH}-th charging cycle, can be obtained from,

$$T_{CH} = \frac{n_{CH}}{f_c}, \quad where\ V_{CP}[n_{CH}] = \sum_{i=1}^{n_{CH}} \Delta V_{CP}[i] = V_{TG} \tag{7.8}$$

The total energy loss in SW_P and SW_N during n_{CH} charging cycles, $E_{SW}[n_{CH}]$, can be calculated as a sum of switching energy losses in each cycle, $\Delta E_{SW}[n]$,

$$\Delta E_{SW}[n] = 2\int_{\frac{n}{f_c}-\frac{1}{4f_c}+t[n]}^{\frac{n}{f_c}+\frac{1}{4f_c}} I_{CH}^2(t) \times R_{SW}\, dt \tag{7.9}$$

$$E_{SW}[n_{CH}] = \sum_{i=1}^{n_{CH}} \Delta E_{SW}[i] \tag{7.10}$$

where R_{SW} is the switch resistance.

The capacitor charging efficiency, η_{CAP}, from L_2 to the C_P and C_N pair of capacitors can be expressed as,

$$\eta_{CAP} = \frac{E_{CP} + E_{CN}}{E_{CP} + E_{CN} + E_{SW}[n_{CH}] + E_{SYS}} \tag{7.11}$$

where E_{CP} and E_{CN} are the stored energy in C_P and C_N, which are $E_{CP} = C_P V_{TG}^2/2$ and $E_{CN} = C_N V_{TG}^2/2$, respectively, and E_{SYS} is the energy consumed by the rest of the system during n_{CH} charging cycles.

Smaller I_{CH} increases T_{CH} in (7.4) - (7.8), while smaller I_{CH} and R_{SW} increase η_{CAP} in (7.9) - (7.11). Therefore, when the maximum tolerable T_{CH} is known, I_{CH} can be selected to be as small as it takes T_{CH} to charge C_P and C_N for C_S and V_{Peak} values in (7.3) - (7.8). C_S should be smaller than C_R, and $V_{Peak} > V_{TG}$.

7.1.3. Implementation of the Inductive Capacitor Charging System

The overall architecture of the proposed capacitor charging system is shown in Fig. 7.5. A power transmitter drives the primary coil, L_1, at the designated carrier frequency, f_c, which induces V_{COIL} across L_2. The capacitor charger consists of switches driven by high-speed active drivers to charge a bank of four pairs of capacitors, C_P and C_N. A control unit sets a user-defined target charging voltage, V_{TG}, and generates a sequence signal, S_{CH}, to operate the 4-channel capacitor charger sequentially, which can be utilized in a programmable multi- electrode neural stimulation [52]. When charging, the capacitor charger connects V_{IN} to positive and negative capacitors alternatively to hold V_{IN} at V_{CP} or V_{CN}, while generating the fixed charging current, I_{CH}, through C_S. In

other words, C_S operates like a current source that does not dissipate power, while reducing the switching loss in the capacitor charger and significantly improving the charging efficiency from L_2 to the capacitor bank.

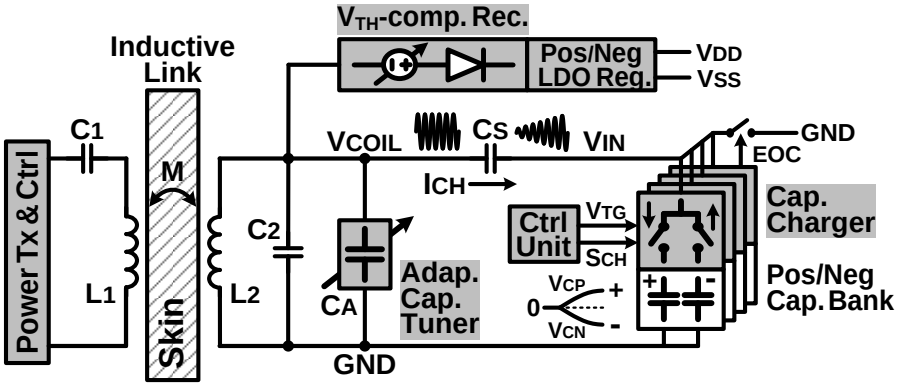


Fig. 7.5. Overall architecture of the proposed power-efficient capacitor charging system through an inductive link.

In this capacitor charging system, the secondary resonance capacitance, C_R, connected across L_2, can be expressed as,

$$C_R = C_2 + C_A + \frac{C_S C_{Eff}}{C_S + C_{Eff}} \tag{7.12}$$

where C_2 is the parallel resonant capacitor, C_A is the adaptive tuning capacitor, and C_{Eff} is the effective capacitance of the capacitor bank, which varies as the capacitor bank voltage and switching duty cycle change. An adaptive capacitor tuner compensates for C_{Eff} variations by automatically adjusting C_A to keep C_R constant. Therefore, the secondary L_2C_2-tank is maintained at resonance during charging, while maximizing V_{COIL}. After the charging cycle, an end-of-charge (EOC) signal connects V_{IN} to *GND*, and the adaptive capacitor tuner is deactivated, setting $C_R = C_2 + C_S$. A dual-output V_{TH}- compensated rectifier followed by low dropout regulators generates the supply voltages, V_{DD} and V_{SS}, from V_{COIL}, which has little effect on the charging operation as long as V_{COIL} amplitude is kept constant by the adaptive capacitor tuner.

Fig. 7.6 shows the schematics of the capacitor charger and one of its active switch drivers. In Fig. 7.6a, if $V_{TG} > V_{CP}$ and S_{CH} = high, the capacitor charger starts charging the

capacitor bank, C_P and C_N, with EN = high. When $V_{IN} > V_{CP}$, the active switch driver, DRV_P, turns on the switch P_1 with V_P = low to provide the positive charging current, $+I_{CH}$, to C_P with a small switch loss.

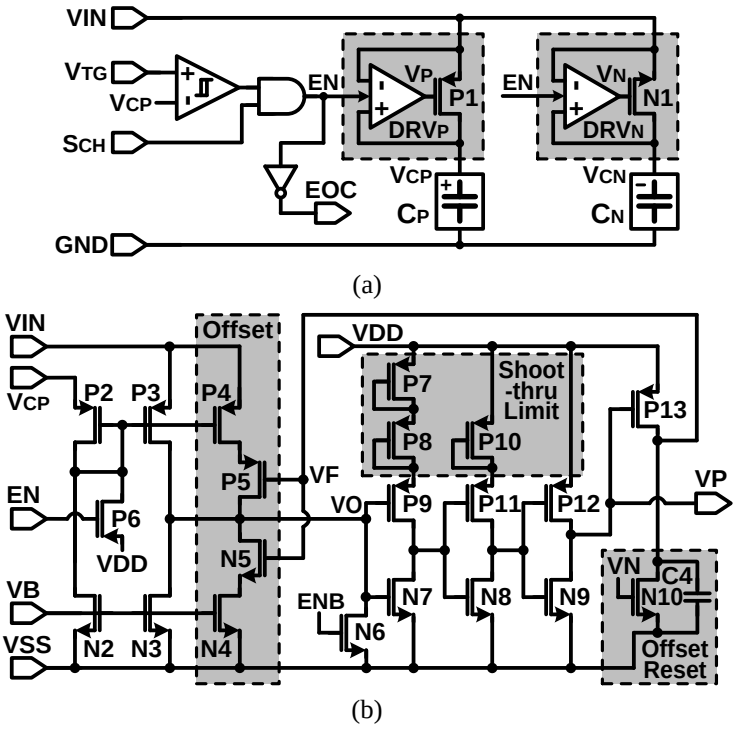


Fig. 7.6. Schematic diagrams of (a) the capacitor charger and (b) one of its active switch drivers, DRV_P.

Fig. 7.6b shows the active switch driver (DRV_P) in which P_2, P_3, N_2, and N_3 form a common-gate comparator, which inputs are connected to V_{CP} and V_{IN}. Since the current drawn from V_{IN} is much smaller than the charging current, it has little effect on the charging operation. An offset block, which consists of current sources, P_4 and N_4, and control switches, P_5 and N_5, injects additional positive or negative offset current depending on a feedback voltage, V_F, to expedite V_O transition for fast P_1 switching, maximize the forward current delivered to the capacitor, and minimize the back current to improve the charging efficiency. Since V_O level depends on V_{IN} amplitude, which varies during charging, shoot-through limited inverters level-shift V_O to supply levels to drive P_1 with proper V_P levels. An offset reset switch, N_{10}, which is driven by V_N, resets the offset by pulling V_F = low after P_1 turns off and $V_{IN} < V_{CN}$ for the next C_P charging cycle. Here,

the timing of the reset signal depends on V_{IN}, which is independent of process variations. DRV_N has a symmetrical structure with respect to DRV_P.

Fig. 7.7 shows the schematic diagram of the adaptive capacitor tuner. A dynamic bias and envelope detector sense the positive V_{COIL} amplitude and compare it to a threshold window around V_{REF} = 1.2 V. If V_{COIL} is outside a designated window (2.7 ~ 2.8 V_P), *UP* or *DN* signals from comparators, CMP_1 or CMP_2, trigger a 7-bit up/down counter to progressively adjust a 7-bit binary-scaled set of tuning capacitors, C_A = 0 ~ 127 × (8 pF), between V_{COIL} and *GND*, to bring V_{COIL} amplitude back within this window. C_A can accommodate the capacitance variations in (7.12), which result from C_S (= 1 nF in this system) in series with C_{Eff} as it varies with $V_{CP,CN}$. The switches for tuning capacitors, P_{17} to P_{23}, are driven by V_{DDH}, which is the higher voltage between V_{DD} and V_{COIL}, to ensure proper turn-off.

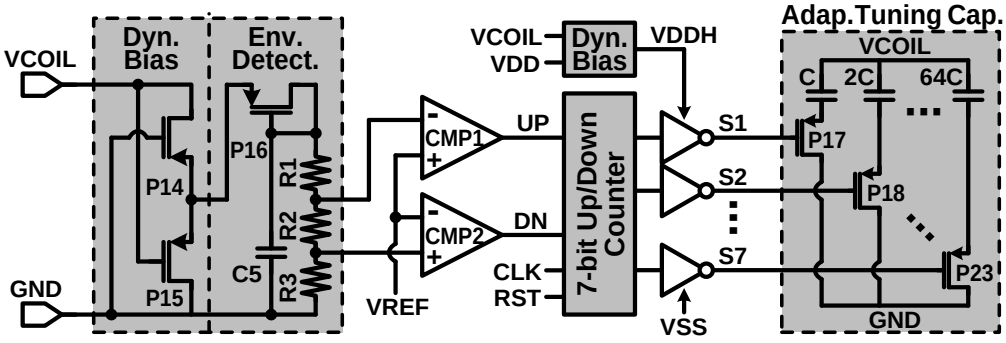


Fig. 7.7. Schematic diagram of the adaptive capacitor tuner.

Fig. 7.8 shows the schematic diagram of the dual-output V_{TH}- compensated rectifier. V_{COIL} is converted to two half-waves, V_{INP} and V_{INN}, to prevent overvoltage across the following transistors that constitute a positive and negative rectifier pair, generating V_{RECP} and V_{RECN}, respectively. In the positive rectifier, $V_{TH(P28)}$ of the diode-connected transistor, P_{28}, compensates for $V_{TH(P27)}$ of the rectifying switch, P_{27}, resulting in a small voltage drop of $V_{GS(P27)}$ - $V_{GS(P28)}$ and high AC-DC power conversion efficiency. R_4 reduces the gate voltage of P_{27} by discharging C_6 in case V_{RECP} decreases.

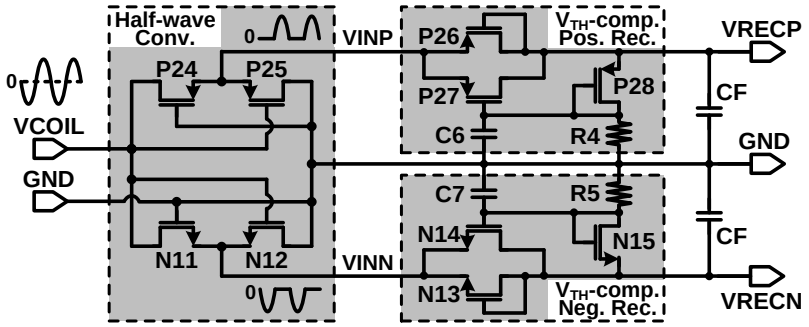
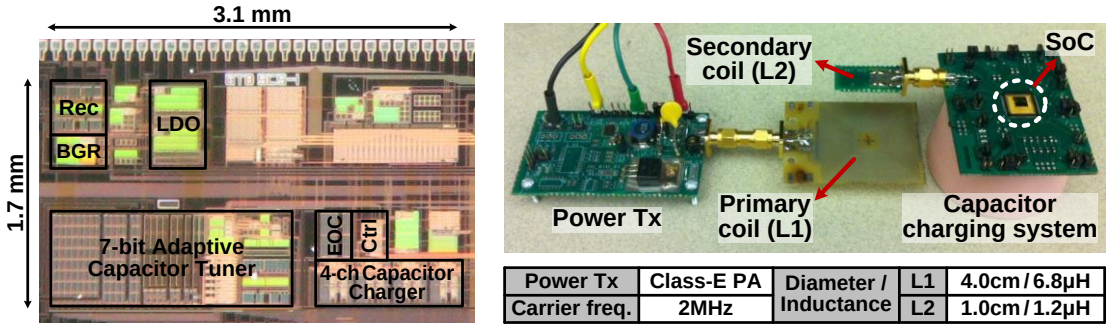


Fig. 7.8. Schematic diagram of the dual-output V_{TH}-compensated rectifier.

7.1.4. Measurement Results

The 4-channel capacitor charging system was fabricated in the TSMC 0.35-µm 4M2P n-well standard CMOS process, occupying 2.1 mm^2. Fig. 7.9 shows the chip micrograph and floor plan of the charging system along with the inductive powering setup. A Class-E power amplifier (PA) on the transmitter side drives the primary coil (L_1 = 6.8 µH and $\varnothing_1$ = 4 cm) at 2 MHz and delivers power across a 15 mm gap to the secondary coil (L_2 = 1.2 µH and $\varnothing_2$ = 1 cm).



(a) (b)

Fig. 7.9. (a) Chip micrograph and (b) testing setup through an inductive link.

Waveforms in Fig. 7.10 show how the capacitor bank is being efficiently charged from V_{COIL}. In Fig. 7.10a, the peaks of V_{IN} follow V_{CP} and V_{CN} traces during charging because the fixed charging current, I_{CH}, results in a small constant voltage drop across the capacitor charger switches, P_1 and N_1. With C_P = C_N = 1 µF, each capacitor pair was charged to V_{CP} = 2 V and V_{CN} = -2 V in 420 µs when V_{COIL} = 2.7 V_P. Fig. 7.10b shows the

active switching waveforms when $V_{CP,CN}$ = 0, ±1, and ±2 V. When $V_{IN} > V_{CP}$, P_1 turns on, holding V_{IN} to V_{CP} plus voltage drop across SW_P, and the voltage across C_S, V_{COIL} - V_{IN}, starts to increase, flowing $+I_{CH}$ into C_P. As V_{CP} increases, the switching duty cycle decreases while the slope of V_{COIL} - V_{IN} remains almost the same, generating a fixed charging current.

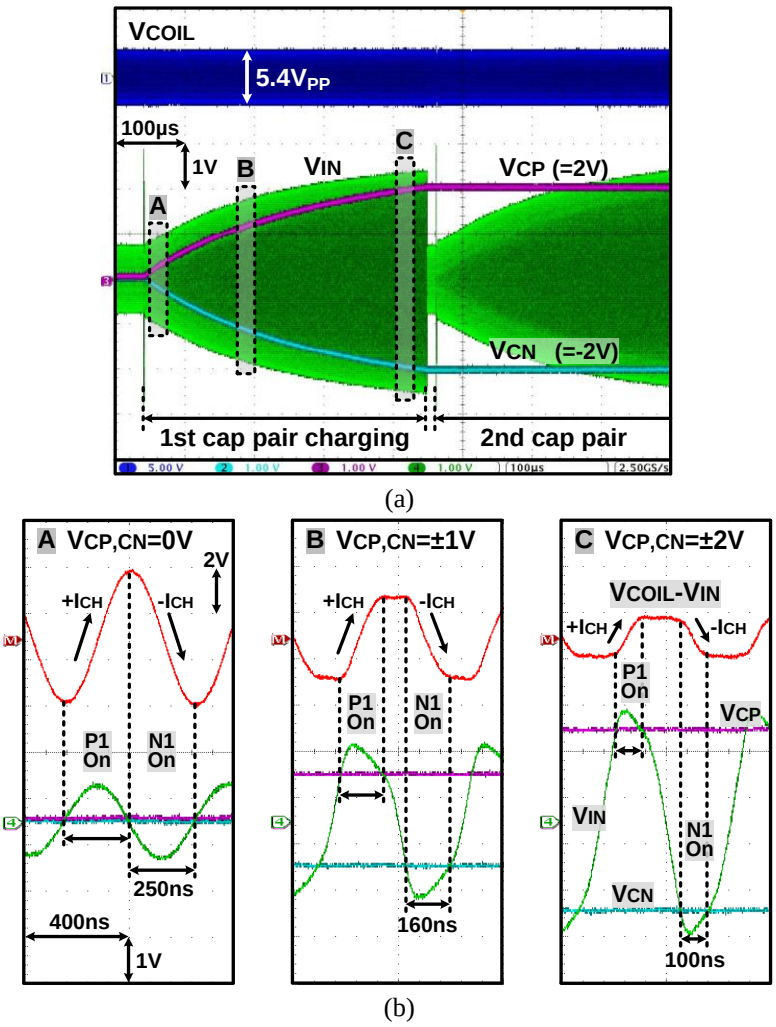
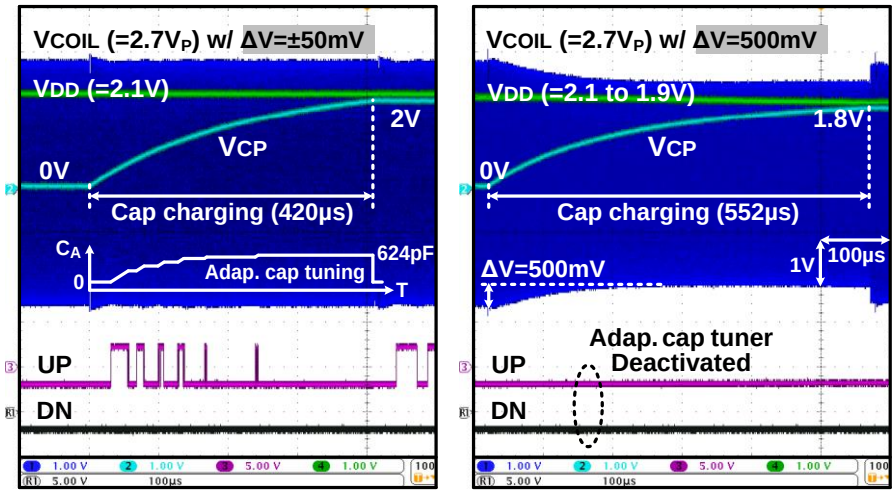


Fig. 7.10. Measured waveforms of (a) the capacitor charger and (b) its zoomed-in switching as $V_{CP,CN}$ of 1 µF capacitor pairs reach ±2 V in 420 µs.

Fig. 7.11 shows how the adaptive capacitor tuner compensates for the C_{Eff} variations and maintains V_{COIL} amplitude constant during charging. In Fig. 7.11a, the *UP* signal triggers the up/down counter, automatically increasing the adaptive tuning capacitor, C_A, to 624 pF as V_{CP} increases. Therefore, C_A compensates for the C_{Eff}

variations, and the secondary resonance capacitance, C_R, in (12) stays at C_2 + C_S during charging, generating a relatively constant V_{COIL} with small ΔV_{COIL} = ±50 mV variations. In Fig. 7.11b, where the adaptive capacitor tuner is deactivated, V_{COIL} amplitude has dropped by 500 mV because of the resonance capacitor detuning, resulting in V_{DD} reduction and limitation of V_{CP} to only 1.8 V, instead of the 2 V target. Therefore, the adaptive capacitor tuner ensures proper charging operation with sufficient V_{COIL} amplitude against C_R detuning.

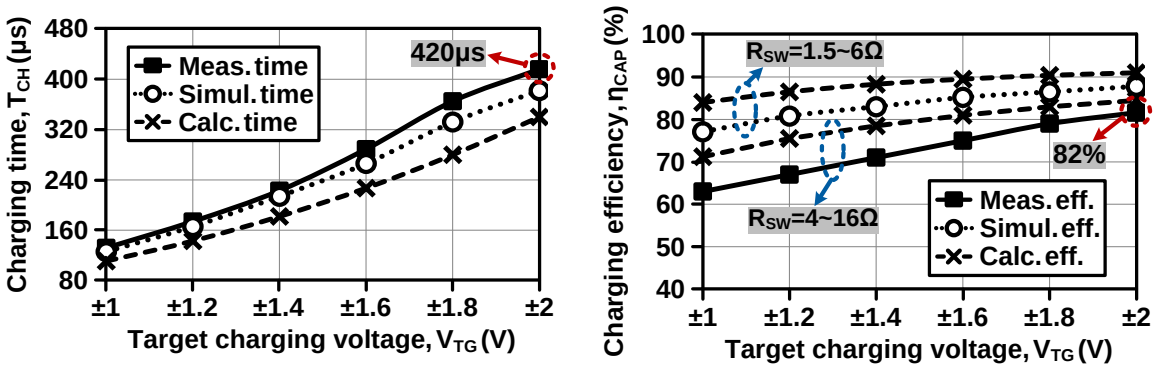


(a) (b)

Fig. 7.11. Measured waveforms of V_{COIL} and $V_{CP,CN}$ variations during capacitor charging (a) with and (b) without the adaptive capacitor tuning mechanism.

Fig. 7.12 shows the measured, simulated, and calculated values of the capacitor charging time and efficiency, while sweeping the target charging voltage, V_{TG}, from ±1 V to ±2 V, to verify the accuracy of our measurement as well as provide insight for further improvements. Calculated charging time and efficiency have been derived from (7.4) - (7.8) and (7.9) - (7.11), respectively, with f_c = 2 MHz, C_S = 1 nF, C_P = C_N = 1 μF, and V_{Peak} = 2.7 V. We assumed that R_{SW} = 1.5 ~ 6 Ω depending on $V_{CP,CN}$ and the system supply power, P_{SYS} = 400 μW, from simulations. In Fig. 7.12a, the 1 μF capacitor pair was charged up to ±2 V in 420 μs. The amount of charging current at each charging cycle gradually decreases as capacitors are charged up because V_{IN} needs longer transition time,

$t[n]$ in (7.6), before charging. Therefore, as the capacitor voltages increase, capacitors require longer charging time for the same amount of voltage increment. Shorter charging time in calculations is the result of the ideal switching of SW_P and SW_N, regardless of $V_{CP,CN}$ levels, which also indicates the maximum possible capacitor charging efficiency.



(a) (b)

Fig. 7.12. Measured, simulated, and calculated (a) capacitor charging time and (b) charging efficiency *vs.* target charging voltage at f_c = 2 MHz, C_S = 1 nF, C_P = C_N = 1 µF, and V_{Peak} = 2.7 V.

In Fig. 7.12b, the charging efficiency was defined as the stored DC energy in the capacitor bank over the total input AC energy of the capacitor charging system. The highest efficiency of 82% was measured when 1 µF capacitors were charged up to V_{TG} = ±2 V. Lower $|V_{CP,CN}|$ increases R_{SW} of P_1 and N_1 switches, leading to larger switching loss and lower charging efficiency as V_{TG} decreases. Discrepancies between measured and simulated efficiencies mainly result from larger R_{SW} of the chip, which was estimated about 4 ~ 16 Ω by observing voltage drops across switches, compared to the simulated R_{SW} = 1.5 ~ 6 Ω. The calculated charging efficiency with R_{SW} = 4 ~ 16 Ω shows closer results to the measured efficiency. While R_{SW} can be further reduced by optimizing the switch sizes, the proposed capacitor charging system achieves high measured charging efficiency of 63 ~ 82% with C_P = C_N = 1 µF charged up to ±1 ~ ±2 V in 132 ~ 420 µs. Table 7.1 summarized the specifications of the inductive capacitor charging system prototype.

Table 7.1: Inductive Capacitor Charging System Specifications

Overall System		**Capacitor Charger**	
Process	0.35 μm CMOS	# of channel	4
L_2 / C_2 / C_S	1.2μH / 4nF / 1nF	Target voltage	±1 ~ ±2 V
Carrier freq.	2 MHz	Charging eff.	63 ~ 82%
Coil distance	1.5 cm	Charging time	132 ~ 420 μs
V_{COIL} peak	2.7 V	C_P / C_N	1 μF / 1 μF
Area	2.1 mm^2	$P_{Supply(Charging)}$	240 μW
Rectifier / Regulator		**Adaptive Capacitor Tuner**	
V_{RECP} / V_{RECN}	2.25 V / -2.25 V	Tuning bit	7-bit
V_{DD} / V_{SS}	2.1 V / -2.1 V	Adaptive cap.	0 ~ 1024 pF
Rec. PCE	72% w/ 50 kΩ	P_{Static}	20 μW*

*Simulation

7.3. A Power-efficient Switched-capacitor Stimulating (SCS) System

7.3.1. SCS System Architecture

Fig. 7.13 shows the overall architecture of the wireless SCS system for head-mounted DBS. The inductive capacitor charger charges four pairs of positive/negative storage capacitors, $C_{P1\sim4}$ and $C_{N1\sim4}$, sequentially, while the adaptive capacitor tuner compensates for the resonance capacitance variation during charging. These capacitors deliver charge to the stimulation sites, which can be either micro-electrode arrays (MEA) or micro-LED arrays, through capacitor/channel selectors for electrical or optical stimulation. For biphasic electrical stimulation, the capacitor pairs are alternately connected to the electrodes, dumping negative and positive charge to the tissue. A current limiter limits the stimulus amplitude to prevent large current flowing through the tissue. To ensure charge-balanced stimulation, a charge monitoring circuit measures the amount of charge injected and withdrawn by observing storage capacitor voltages, and dynamically changes the stimulus pulse width to neutralize the residual charge in the tissue. An additional charge balancing circuit further prevents residual charge accumulation by shorting electrodes to ground for predefined time after stimulation. A power management block generates positive and negative system supply voltages and reference voltages, while a timing controller provides timing signals for capacitor

charging and charge-based stimulation. In forward data telemetry, a pulse-position-modulated clock/data recovery (PPM-CDR) extracts synchronized data and clock from an on-off-keying (OOK) modulated coil voltage, V_{COIL}, setting a 40-bit shift register through a serial-to-parallel converter (S2P) with 8-bit preambles, to store stimulation parameters. Load-shift-keying (LSK) back telemetry has been adopted for forward telemetry handshaking and closed-loop power control by sensing V_{COIL} amplitude.

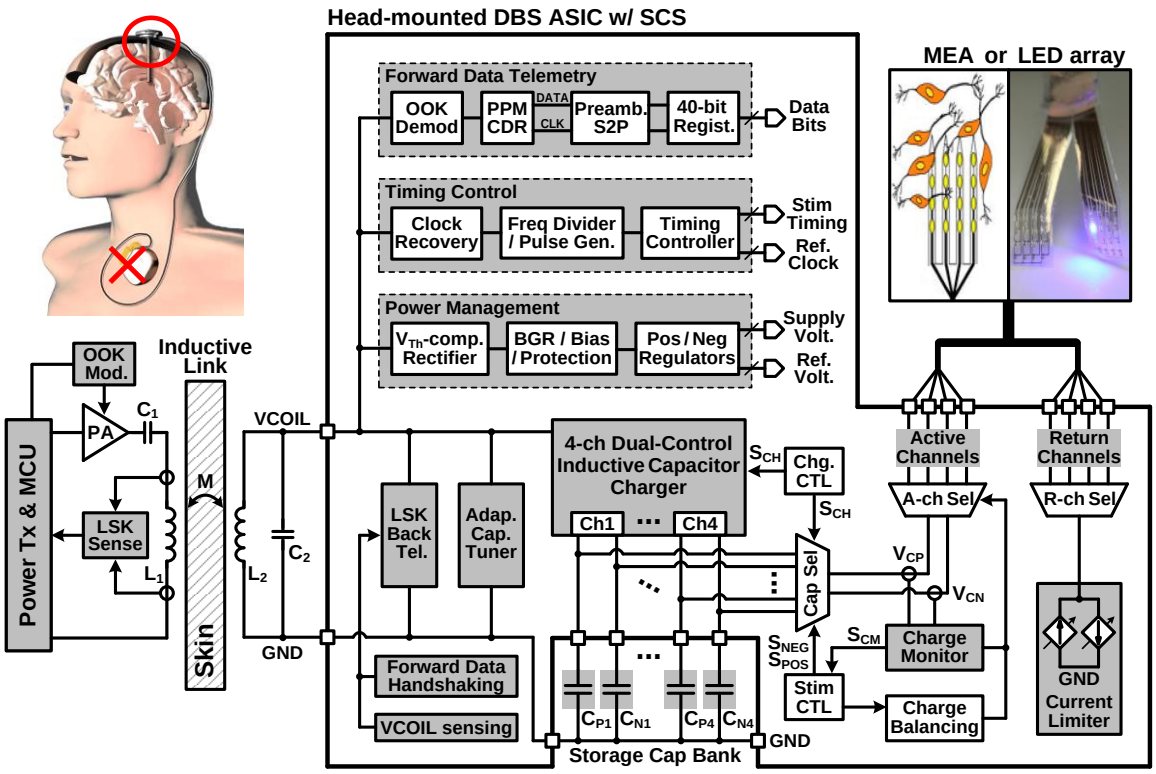


Fig. 7.13. Overall architecture of the integrated wireless SCS system for head-mounted DBS.

The decaying-exponential shape of the current stimulus can be adjusted by changing stimulation parameters that are set through the forward telemetry. Fig. 7.14 shows the simplified SCS system and electrodes/tissue model to analyze the decaying-exponential current stimulus. The electrodes/tissue model includes a series R_S and C_{DL}, which represent the solution spreading resistance and the double-layer capacitance, respectively [79], [80].

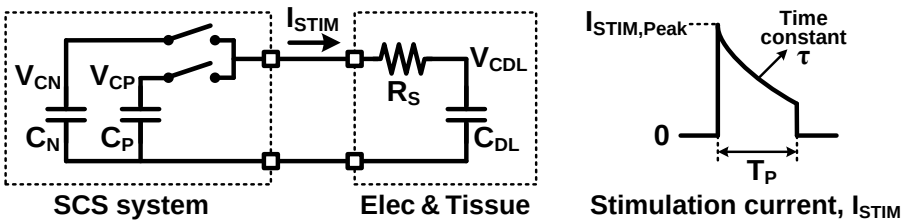


Fig. 7.14. Simplified SCS system and electrode/tissue model.

Assume that storage capacitors, C_P and C_N, are charged to target voltages, V_{TP} and V_{TN}, respectively, and C_{DL} is discharged to 0 V. When C_P is connected, the stimulation current, I_{STIM}, flows to the tissue through electrodes. During the positive stimulation, V_{CP}, V_{CDL}, and I_{STIM} can be expressed as,

$$\mathrm{V_{CP}}(t) = \mathrm{V_{TP}} - \frac{1}{\mathrm{C_P}}\int \mathrm{I_S}(t)\mathrm{d}t \tag{7.13}$$

$$\mathrm{V_{CDL}}(t) = \frac{1}{\mathrm{C_{DL}}}\int \mathrm{I_S}(t)\mathrm{d}t \tag{7.14}$$

$$\mathrm{I_{STIM}}(t) = \frac{\mathrm{V_{CP}}(t) - \mathrm{V_{CDL}}(t)}{\mathrm{R_S}} = \frac{\mathrm{V_{TP}} - \left(\frac{1}{\mathrm{C_P}} + \frac{1}{\mathrm{C_{DL}}}\right)\int \mathrm{I_S}(t)\mathrm{d}t}{\mathrm{R_S}} \tag{7.15}$$

Then, I_{STIM} can be derived further as,

$$\mathrm{I_{STIM}}(t) = \frac{\mathrm{V_{TP}}}{\mathrm{R_S}} exp\left(-\left(\frac{1}{\mathrm{C_P}} + \frac{1}{\mathrm{C_{DL}}}\right)\left(\frac{1}{\mathrm{R_S}}\right)t\right)$$

$$= \frac{\mathrm{V_{TP}}}{\mathrm{R_S}} exp\left(-\frac{\mathrm{t}}{\frac{\mathrm{C_P C_{DL}}}{\mathrm{C_P + C_{DL}}}\mathrm{R_S}}\right) = \frac{\mathrm{V_{TP}}}{\mathrm{R_S}} exp\left(-\frac{\mathrm{t}}{\tau}\right) \tag{7.16}$$

From (7.16), the peak stimulation current, $I_{STIM,Peak}$ (= V_{TP} / R_S), and the time constant of decaying exponential, τ, can be adjusted by changing the target charging voltage, V_{TP}, and the number of storage capacitors connected to the tissue (= C_P x n), respectively. The positive stimulation period, T_P, can be also controlled through forward telemetry, enabling flexible shapes of decaying-exponential current stimulus as shown in Fig. 7.14. The negative stimulation current can be adjusted in the same way with V_{TN}, C_N, and T_N.

7.3.2. Circuit Details and Design Considerations

Since capacitor charging efficiency is a dominant factor in stimulator efficiency, we utilized the power-efficient inductive capacitor charging concept in chapter 7.2 plus additional safety features for SCS. Fig. 7.15 shows the schematic diagram of the improved 4-channel inductive capacitor charger. A coil voltage, V_{COIL}, is followed by a series charge injection capacitor, C_S, which provides an input voltage, V_{IN}, to C_{P1} and C_{N1} through switches P_1 and N_1, respectively. When $V_{CP1} < V_{IN} < V_{CN1}$, both switches turn off, and V_{IN} follows V_{COIL}. Then, when either P_1 or N_1 turns on by a switch driver, DRV_P or DRV_N, the switch connects V_{IN} to positive or negative capacitor voltage, V_{CP1} or V_{CN1}, holding V_{IN} relatively constant. Since V_{COIL} keeps increasing or decreasing, the voltage difference across C_S generates a fixed charging current to the storage capacitors. In other words, C_S operates like a current source that does not dissipate power, while reducing switching loss and improving charging efficiency from the inductive link to capacitors.

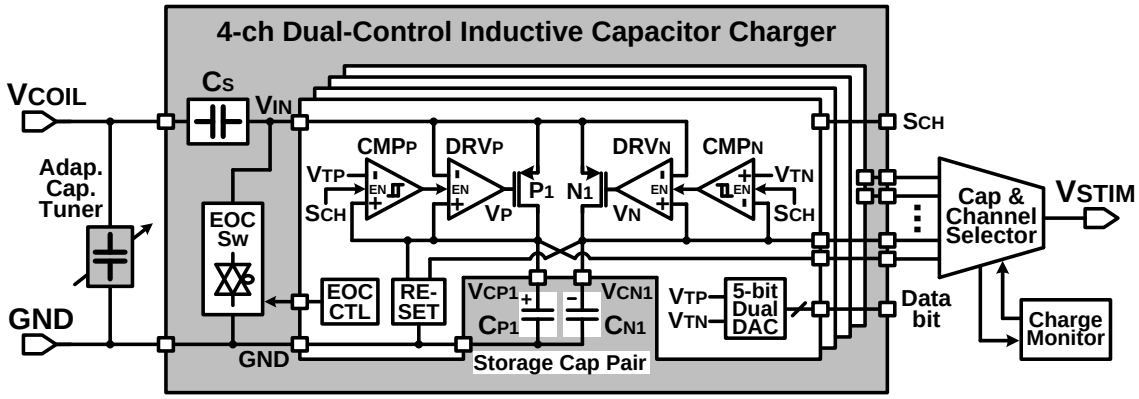


Fig. 7.15. Schematic diagram of the 4-channel dual-control inductive capacitor charger.

The improved charger benefits from dual-voltage control capability provided by comparators, CMP_P and CMP_N, and a 5-bit dual-output DAC to guarantee that V_{CP1} and V_{CN1} are separately charged to target voltages, V_{TP} and V_{TN}, respectively. Otherwise, even small residual voltage mismatch between C_{P1} and C_{N1} can be accumulated during long-term stimulation and saturate either V_{CP1} or V_{CN1}. There is also a reset function that can optionally discharge C_{P1} and C_{N1} before charging. While the 4-channel capacitor charger

operates sequentially, the end-of-charge (EOC) switch connects V_{IN} to *GND* after charging. In addition, the adaptive capacitor tuner adopted from chapter 7.2 automatically compensates for variations of secondary resonance capacitance during charging.

For accurately charge-balanced biphasic stimulation, we have utilized the charge monitoring circuit as shown in Fig. 7.16. The charge monitoring circuit utilized a capacitive-feedback amplifier to integrate the discharged voltages from storage capacitor voltages, V_{CP} and V_{CN}, during stimulation to detect the amount of negative and positive charge transferred to tissue. A charge monitoring signal, S_{CM}, stays at 0 before stimulation, while amplifiers A_1 and A_2 operate as buffers, storing their offset voltages in C_5. When the negative stimulation starts first with S_{CM} = 1 for a predefined period, A_1 becomes a capacitive-feedback amplifier, and A_2 operates as a comparator, while their offsets are cancelled through C_5. A sensing voltage, V_{SEN}, decreases as V_{CN} increases in this period. When V_{CP} discharges for positive stimulation, V_{SEN} increases again. When the amounts of V_{SEN} decrement and increment are equal, S_{CM} = 0 again, and the positive stimulation stops to ensure that the net injected and withdrawn charges are zero.

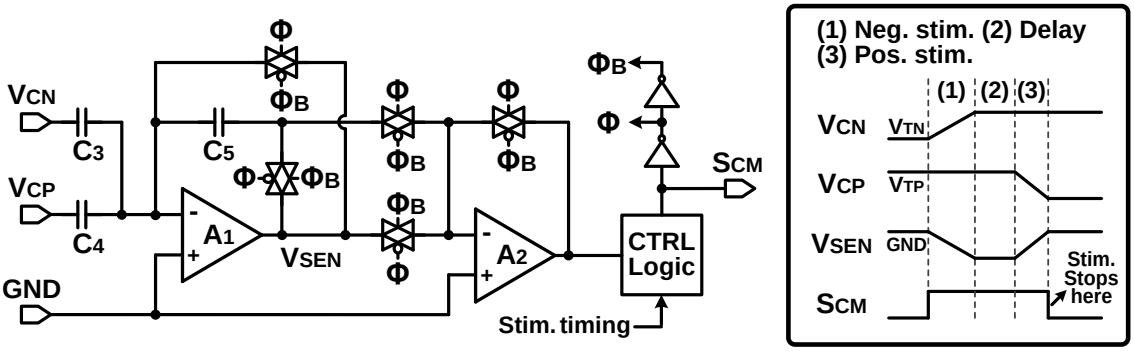


Fig. 7.16. Schematic diagram of the charge monitoring circuit.

Fig. 7.17 shows the schematics of the OOK demodulator and PPM-CDR. In the OOK demodulator, V_{COIL} is converted to a half wave through P_2 and P_3 to prevent overvoltage across a following diode-connected rectifying transistor, P_4. Then, the envelope of V_{COIL} is extracted through P_4 and a hysteresis comparator, A_3, to provide a pulse-position-modulated (PPM) signal, S_{PPM}. In the PPM-CDR, S_{PPM} is converted to the

clock, *CLK*, through a frequency divider (DFF_1). *CLK* controls the timing and amplitude of V_{PPM} by alternately charging and discharging C_7 through current sources, I_2 and I_3, respectively. If positioning ratio among three pulses of S_{PPM} is 7:3, I_2 charges C_7 for longer time, and V_{PPM} exceeds a reference voltage, V_{REF2}, during *CLK* = 1. Then, a demodulated signal, S_{PPD}, is sampled in DFF_2, leading to *DATA* = 1. On the contrary, when the positioning ratio is 3:7, V_{PPM} does not reach to V_{REF2} during *CLK* = 1, resulting in *DATA* = 0. Since the stimulation parameters are set only once and the OOK pulse width is narrow (3μs), the OOK-PPM offers a simple but robust programming method without costing the system efficiency.

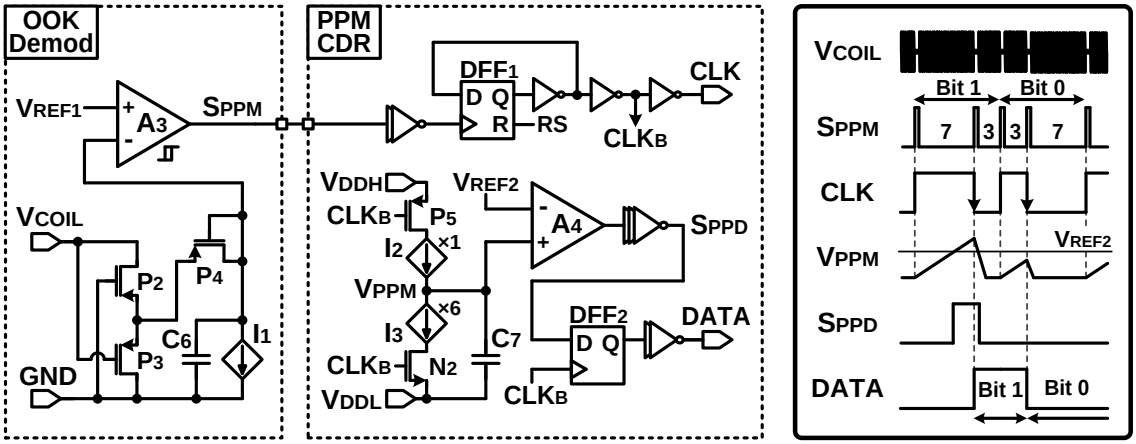


Fig. 7.17. Schematic diagrams of the OOK demodulator and PPM-CDR.

In addition, the LSK back telemetry has been utilized for the closed-loop power control to accommodate with a wider range of mutual coil arrangement. An external power transmitter (Tx) in Fig. 7.13 increases the transmitted power by default with an adjustable step size unless detecting the back telemetry data. When the envelope of V_{COIL} exceeds a certain threshold, the V_{COIL} sensing block sends short pulses (1.5 μs) at 500 Hz to the LSK block, closing the switch across the secondary coil, L_2. Then, the voltage increment across the primary coil, L_1, is detected by the external LSK sensing block, and the power Tx decreases the transmitted power until no more back telemetry data are received, keeping V_{COIL} amplitude at a desired level against coil misalignments.

7.3.3. Electrical Stimulation Measurement

The 4-channel wireless SCS system was fabricated in the TSMC 0.35-μm 4M2P standard CMOS process, occupying 12 mm^2 including pads. Fig. 7.18 shows the chip micrograph and floor plan of the wireless SCS system.

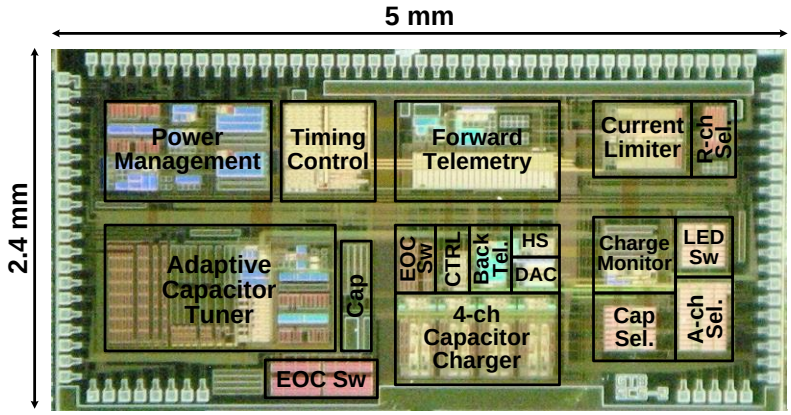
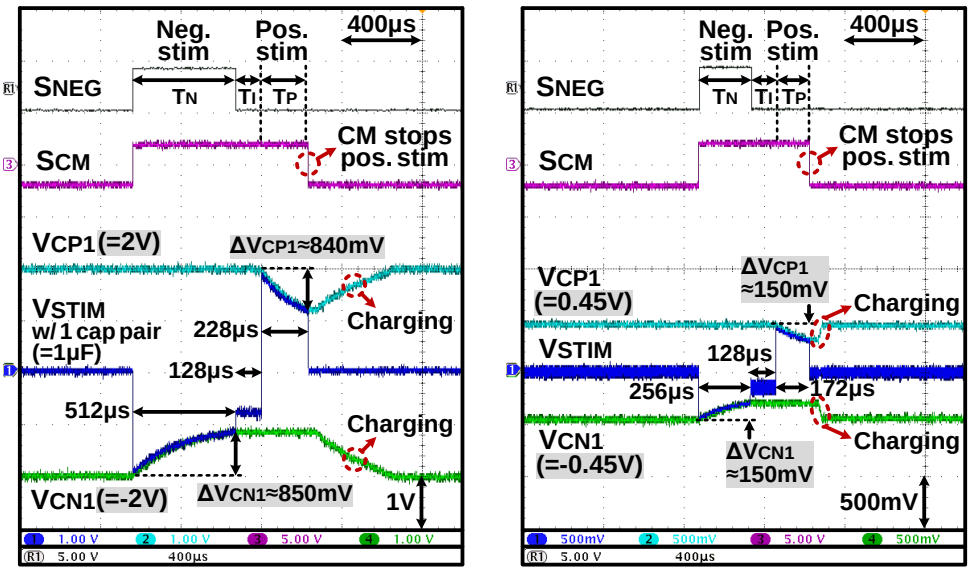


Fig. 7.18. Fabricated chip micrograph of the wireless SCS system.

Measured waveforms in Fig. 7.19 show the operation of charge monitoring (CM) circuit while changing the storage capacitor voltages, V_{CP1} and V_{CN1}, and the negative stimulation period, T_N. A negative-first biphasic stimulation voltage, V_{STIM}, flows through a series *RC* model (500 Ω and 1 μF) for the DBS application [58], [82]. In Fig. 7.19a, the negative stimulation is applied for predefined 512 μs with one ±2 V capacitor pair, discharging V_{CN1} by 850 mV. Then, the positive stimulation period, T_P, is dynamically adjusted to 228 μs by the charge monitoring circuit, discharging the same amount of ΔV_{CP1} to ensure that injected and withdrawn charges are neutralized. Similarly, when T_N = 256 μs with one ±0.45 V capacitor pair in Fig. 7.19b, the positive stimulation is provided for T_P = 172 μs to discharge ΔV_{CP1} = 150 mV, leading to charge balancing.

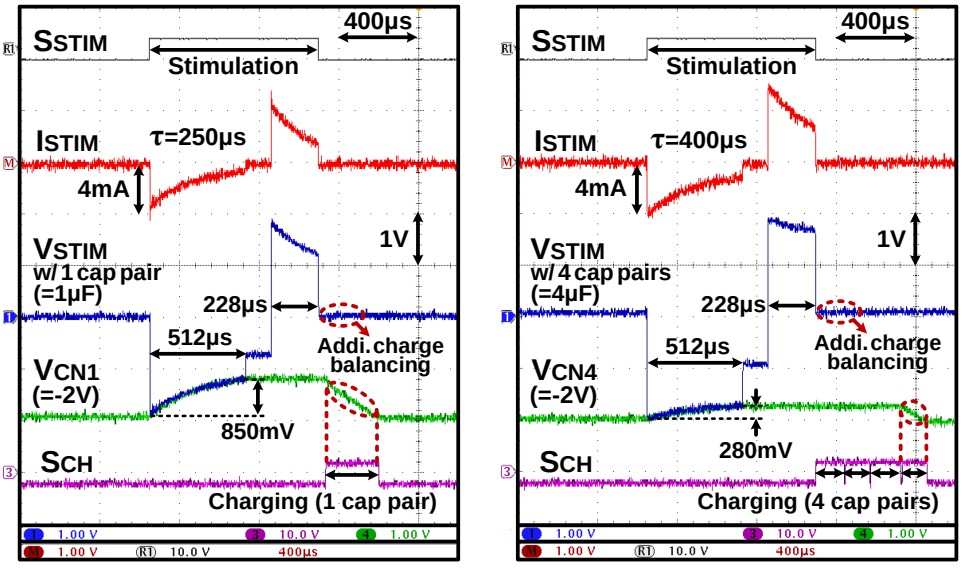
Fig. 7.20 shows the overall SCS waveforms focusing on stimulation with different number of storage capacitor pairs. In Fig. 7.20a, one capacitor pair charged to ±2 V provides the stimulation current, I_{STIM}, with a decaying-exponential shape, and its amplitude (= 4 mA) and time constant (= 250 μs) depend on storage capacitors (= 1 μF), electrodes/tissue *RC* (= 500 Ω and 1 μF), and $V_{CP,N}$ (= ±2 V target) as analyzed in (7.16).

With four capacitor pairs in Fig. 7.20b, the time constant of I_{STIM} increases to 400 µs, while smaller voltage of 280 mV is discharged from each capacitor. After stimulation, capacitor pairs are sequentially charged to target voltages again, while the site is shorted to *GND* during a predefined period for additional charge balancing.



(a) (b)

Fig. 7.19. Measured waveforms of the charge monitoring circuit with (a) V_{CP1} = 2 V, V_{CN1} = -2 V, and T_N = 512 µs and (b) V_{CP1} = 0.45 V, V_{CN1} = -0.45 V, and T_N = 256 µs.



(a) (b)

Fig. 7.20. Measured waveforms of the overall SCS system focusing on stimulation with (a) one capacitor pair and (b) four capacitor pairs.

Fig. 7.21 shows the measured waveforms of forward/back data telemetry. In Fig. 7.21a, V_{COIL} was OOK-demodulated to the pulse-position-modulated signal, S_{PPM}, which is converted to synchronized 15.6 kbps data and clock by PPM-CDR. Then, the recovered 40-bit data are sampled by S2P and stored in shift registers. After receiving the forward data, the handshaking block generates two short pulses (2 μs), which are provided to the external power Tx through LSK back telemetry for handshaking. Fig. 7.21b shows the closed-loop power control capability with LSK back telemetry. When the positive rectifier output voltage, V_{RECP}, exceeds the closed-loop target voltage of 2.3 V, the V_{COIL} sensing block provides a back telemetry signal, S_{BT}, with 1.5 μs pulse width at 500 Hz to close the LSK switch across L_2. Then, a sudden drop in V_{COIL} increases the secondary quality factor, Q_2, and the primary coil voltage, V_{L1}, by 5 V_{PP}, which is detected by the LSK sensing block.

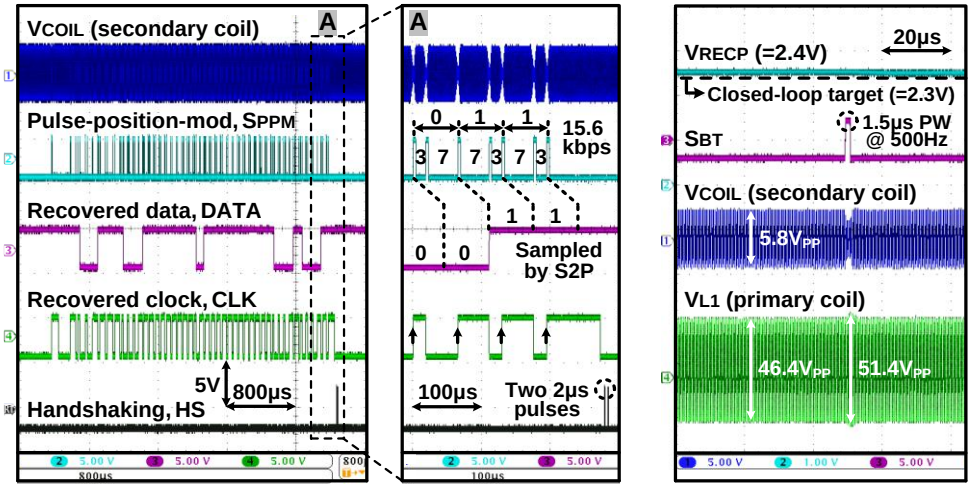


Fig. 7.21. Measured waveforms of (a) the forward data telemetry and (b) back data telemetry.

In order to verify the accuracy of the charge monitoring circuit, we measured the discharged voltage mismatch between negative and positive capacitors, C_N and C_P, for biphasic stimulation while calculating the residual charge in the tissue. Fig. 7.22a shows the measured discharged voltage of C_N (= ΔV_{CN}) and the mismatch between discharged voltages of C_N and C_P (= ΔV_{CN} - $|\Delta V_{CP}|$) during stimulation, while sweeping capacitor

voltages, V_{CP} and V_{CN}, from ±0.45 V to ±2 V. The discharged voltage mismatch was measured between 14 mV and 22 mV. Fig. 7.22b shows the residual charge, ΔQ_{STIM}, vs. $V_{CP,N}$ in the tissue after stimulation, which was derived from,

$$\Delta Q_{STIM} = |Q_{NEG}| - Q_{POS} = |C_N \Delta V_{CN}| - C_P \Delta V_{CP} \quad (7.17)$$

where Q_{NEG} and Q_{POS} are injected and withdrawn charges during negative and positive stimulation, respectively, and $C_N = C_P = 1$ µF. While the maximum residual charge was 22 nC with 512 µs negative stimulation period, the minimum charge ratio between ΔQ_{STIM} and Q_{NEG} was 2.2% when $V_{CP,N} = \pm 2$ V.

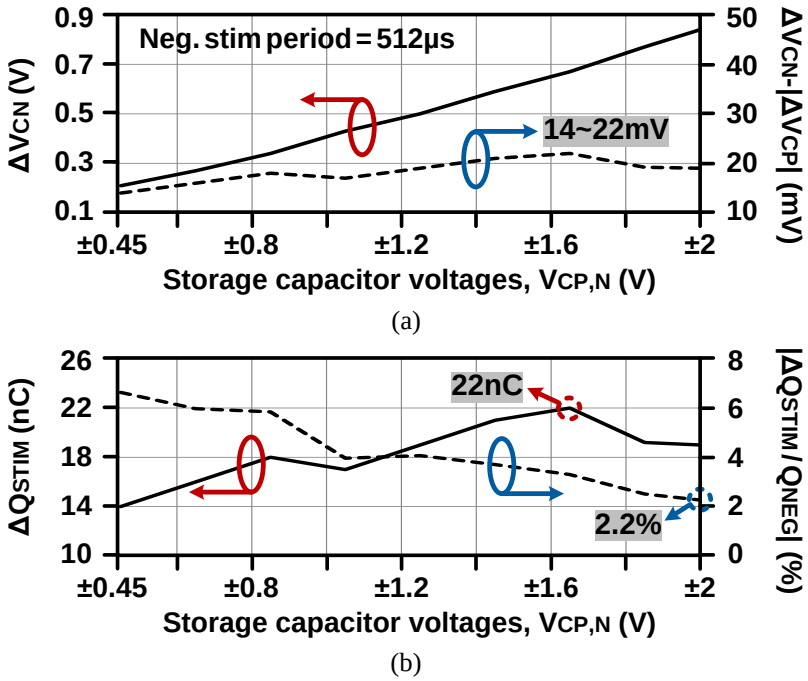


Fig. 7.22. (a) Measured discharged voltage mismatch between negative and positive capacitors, ΔV_{CN} - ΔV_{CP}, during biphasic stimulation, and (b) the residual charge, $\Delta Q_{STIM} = |Q_{NEG}| - Q_{POS}$, in the tissue, while sweeping capacitor voltages, $V_{CP,N}$.

INL and DNL of the 5-bit storage capacitor voltages, V_{CP} and V_{CN}, with dual-control inductive capacitor charging were measured and presented in Fig. 7.23 along with the charged voltage mismatch, $\Delta V_{CH} = |V_{CN}| - V_{CP}$. While V_{CP} and V_{CN} were charged from ±0.45 V to ±2 V with 5-bit resolution, the maximum INL and DNL were 0.44 LSB and 0.24 LSB, respectively. The maximum ΔV_{CH} between $|V_{CN}|$ and V_{CP} was ±26 mV.

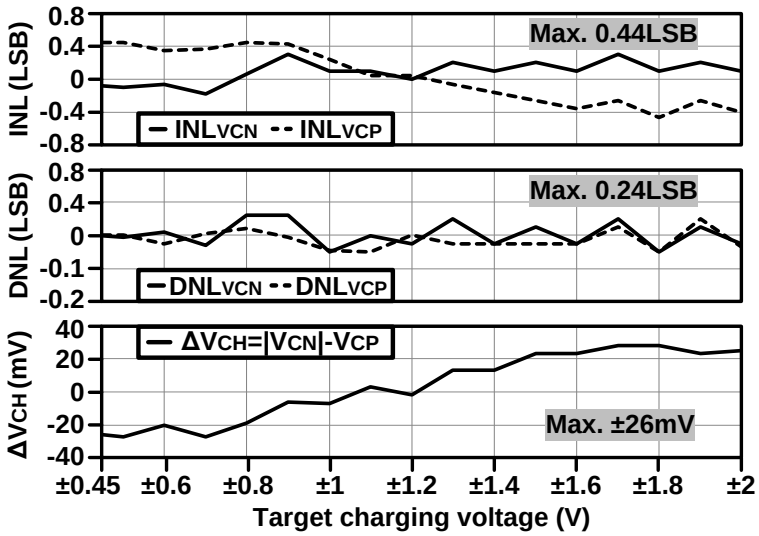


Fig. 7.23. Measured INL and DNL of the 5-bit storage capacitor voltages, V_{CN} and V_{CP}, along with the charging voltage mismatch, $\Delta V_{CH} = |V_{CN}| - V_{CP}$.

7.3.4. Performance Comparison and Summary

Table 7.2 benchmarks the proposed wireless SCS system against several state-of-the-art stimulating systems.

Table 7.2: Inductively Powered Stimulating System Benchmarking

Publication		2010 [47]	2012 [58]	2011 [54]	**This work**
Technology		0.18µm HV	0.35µm	1.5µm	**0.35µm**
Stimulator structure		CCS	VCS + CCS	SCS	**SCS**
Supply voltage (V)		±12	3.3	±1.75 (Cap)	**±2 (Cap)**
Stimulator power efficiency (%)	Rec. + Reg.	85.6	80*	-	**-**
	DC-DC conv.	-	55 ~ 94	-	**-**
	Current driver	41.6	-	-	**-**
	Charger + Sw.	-	-	40**	**80.4**
	Total	35.6	44 ~ 75.2	40	**80.4**
Current stimulus shape		Rectangular	Rectangular	Decaying exponential	**Decaying exponential**
Max. I_{STIM} (mA)		0.5	0.45	0.4 (peak)	**4 (peak)**
Series *RC* model		10kΩ + 100nF	1kΩ + 0.93µF	1.15kΩ + 0.98µF	**0.5kΩ + 1µF**

* With the rectifier only, ** Including power consumption of other blocks.

Inductively powered stimulating systems, which utilized CCS or VCS, require the rectifier, regulator, current driver, and even DC-DC converter to generate rectangular stimuli, while power losses at each stage result in poor stimulator efficiencies. The stimulating system in [54] adopted switched-capacitor stimulation to utilize decaying-

exponential stimuli, but it suffers from poor capacitor charging efficiency. The proposed wireless SCS system can achieve high stimulator efficiency of 80.4% when ±2 V capacitor pair provides the decaying-exponential stimulus to the tissue thanks to the power-efficient dual-control inductive capacitor charger and low-resistance capacitor/channel selectors. In addition, our SCS system enables flexible decaying-exponential shapes by adjusting stimulation parameters through forward telemetry, while injected and withdrawn charges are monitored and balanced for safe stimulation. Table 7.3 summarizes the specifications of the power-efficient 4-channel wireless SCS system.

Table 7.3: Wireless SCS System Specifications

Overall System		**Switched-capacitor stimulation**	
L_1 / L_2 / f_C	4 μH / 1.2 μH / 2 MHz	# of channels	4 (active) + 4 (return)
ASIC area	12 mm^2	Stimulation freq.	7.6 ~ 244 Hz (5-bit) *
System supply	2.1 V / -2.1 V	Pulse width	16 ~ 512 μs (5-bit)*
Inductive capacitor charger		Charge balancing	Charge monitor + passive
Target voltages	±0.45 ~ ±2 V (5-bit)	$\|Q_{NEG}\|$ - Q_{POS}	< 22 nC with $C_{P,N}$ = 1 μF
INL / DNL	0.44 / 0.24 LSB	Current limiter	0.012 ~ 1.5mA (5-bit)**
$\|V_{CN}\|$ - V_{CP}	< ±26 mV	**Forward data telemetry**	
Charging eff. / time	45 ~ 82% / 40 ~ 420 μs	Data / Preamble bits	40 / 8 bits
C_S / $C_{P1\sim4}$ / $C_{N1\sim4}$	1 nF / 1 μF / 1 μF	PPM data rate	15.6 kbps

* Adjustable, ** No limiting option available.

7.3.5. Wireless Optogenetics with SCS

The proposed SCS system is capable of providing high instantaneous current through storage capacitors without degrading the inductive link coupling and system supply voltages, which are limiting factors in conventional inductively powered devices. Therefore, we have utilized the wireless SCS system for power-efficient optogenetics by periodically discharging the storage capacitors into micro-LED arrays, which requires high instantaneous power to emit sufficient light and evoke the neural activity [95]. Fig. 7.24 shows the conceptual diagram of the wireless SCS system which efficiently charges storage capacitors, C_P and C_N, while being capable of driving micro-LEDs with high instantaneous current. After charging, C_P and C_N pairs are connected in series to provide higher LED voltage, V_{LED}, for optical stimulation.

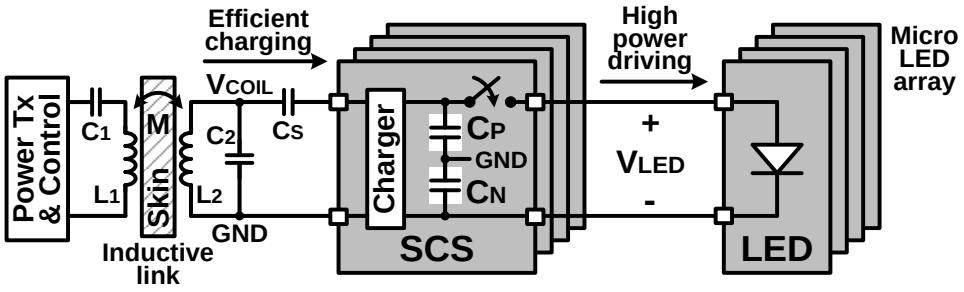


Fig. 7.24. Conceptual diagram of the wireless SCS system for power-efficient optogenetics with micro-LED arrays.

Fig. 7.25 shows the 3D model for *in vivo* wireless optogenetics with the SCS system which receives wireless power and data through the inductive link. The SCS ASIC drives the 3D flexible optrode array, which consists of micro-LEDs for optical stimulation and transparent penetrating electrodes for neural recording, while micro-needle waveguides enable precise and efficient light delivery to the target tissue with high spatial resolution [96]. The neural signals are recorded using a commercial setup (RHD2132, Intan Technologies, Los Angeles, CA) from the penetrating electrodes, which are wrapped around the waveguide core and only exposed at the tips of the waveguides. Therefore, the wireless SCS system with slanted optrode arrays enables simultaneous optical stimulation and electrical neural recording for untethered bi-directional neural interface.

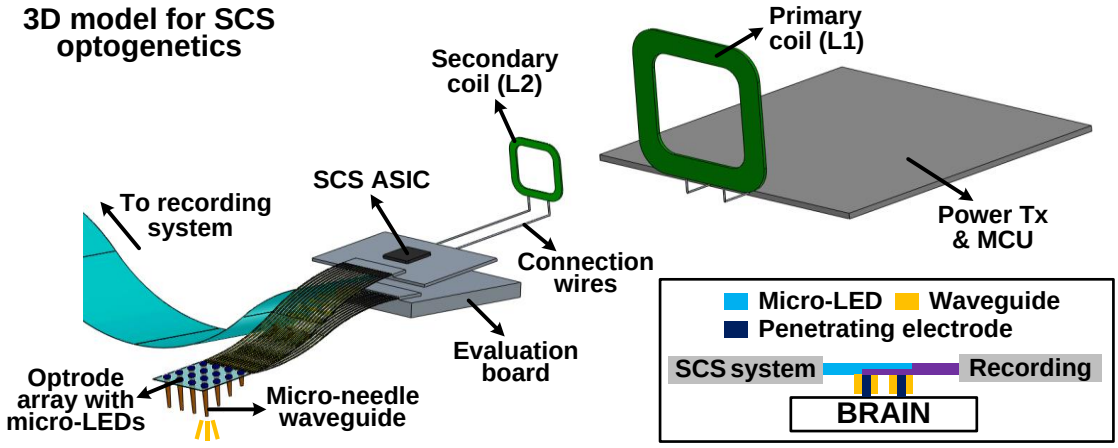


Fig. 7.25. 3D model for *in vivo* optogenetics experiments with the SCS system. Inset: Optrode array with micro-LEDs for optical stimulation and transparent penetrating electrodes for neural recording.

CHAPTER VIII

IN VIVO ANIMAL EXPERIMENTS WITH THE SCS SYSTEM

8.1. Energy-efficient Stimulus Waveform

8.1.1. Tissue Model

In addition to high stimulator efficiency, the proposed switched-capacitor stimulating (SCS) system is capable of generating the decaying-exponential current stimulus by dumping charge in capacitors to the tissue without consuming additional power, while the decaying-exponential stimulus is proven to be more effective in activating the neural tissue compared to rectangular and ramp stimuli depending on the stimulus pulse width when consuming same amount of energy [61], [62]. To verify the energy-efficient stimulus waveform shape, we modeled the tissue with axons and simulated the effects of stimulus waveforms to the area of tissue activated.

Fig. 8.1 shows the multi-compartment double-cable model of a mammalian axon and its finite-element model, which were adopted from [97]. In Fig. 8.1a, the myelinated axon model consists of 21 nodes of Ranvier separated by 20 internodes. Since most of axon areas are covered by the myelin sheath, only the nodes of Ranvier are affected by the extracellular potential and generate the action potential. Typically, axons with larger diameter tend to be myelinated (covered by a myelin sheath), which allows the axons to conduct action potentials at greater velocities than unmyelinated axons with smaller diameter (not covered by a myelin sheath). In Fig. 8.1b, each node of Ranvier can be represented with the Hodgkin and Huxley (HH) model as a nodal compartment, while the internodal segments (FLUT and STIN) include the resting potential, V_{rest}, conductance, G_i, and capacitance, C_i. These internodal segments are covered by the myelin sheath, which is represented as G_m and C_m. The nodes of Ranvier and the internodal segments are connected through the conductance, G_a and G_p, which mean the axoplasmic and periaxonal conductance, respectively.

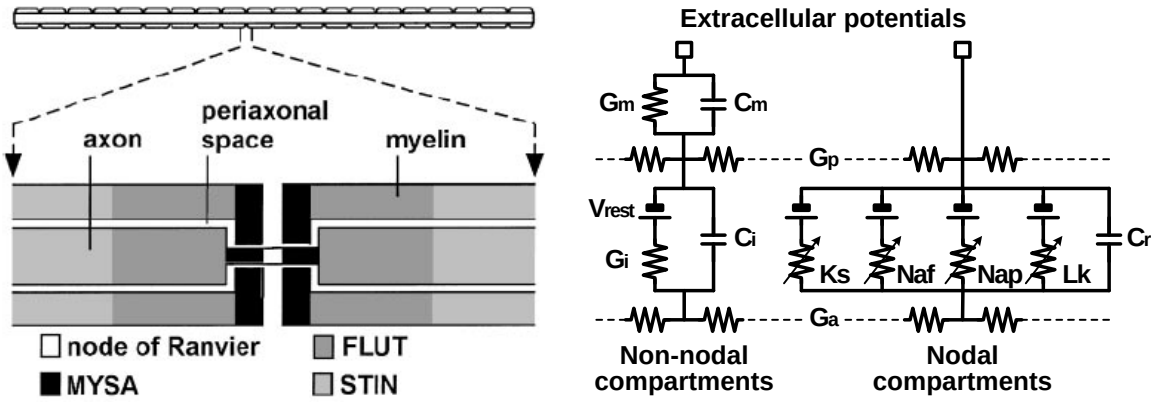


Fig. 8.1. (a) Multi-compartment double-cable mammalian axon model. (b) Finite-element axon model [97].

Geometric and electrical parameters of the axon model in Fig. 8.1 have been also adopted from [97]. For the tissue modeling here, the geometric parameters of the axon fiber with 5.7 μm diameter were used. In this case, the length and diameter of the node of Ranvier are 1 μm and 1.9 μm, respectively. With the surface area of the node of Ranvier, the electrical parameters of the axon model can be calculated.

Fig. 8.2 shows the finite-element schematic of the double-cable axon array with 11 nodes of Ranvier for Cadence simulation (Cadence Design System Inc., San Jose, CA). While various shapes of stimulus waveforms from the stimulation electrode change the potentials in the tissue, these extracellular potentials will be applied to each node of Ranvier to increase the transmembrane potential and evoke neural responses.

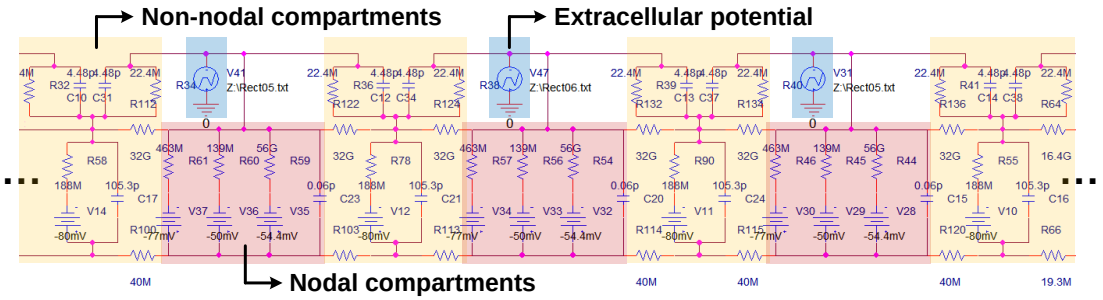


Fig. 8.2. Finite-element schematic of the double-cable axon array for Cadence simulation.

In this modeling, 11 nodes of Ranvier were designed and simulated instead of 21 nodes for simplicity of the simulation. In [98], Warman and Grill analyzed the effect of

the extracellular potential and intracellular current from neighboring nodes of Ranvier. The results showed that the errors of the extracellular stimulation that come from outside of 6th neighboring nodes can be negligible (< 1%). Therefore, using 11 nodes of Ranvier will guarantee the accuracy of the model while offering simple simulation steps.

Fig. 8.3 shows the conceptual tissue model with a stimulation electrode and axon arrays. For extracellular stimulation, tissue potentials that vary depending on stimulus waveforms from the stimulation electrode were calculated along the length of each axon by using COMSOL simulation (COMSOL Inc., Burlington, MA). Then, the extracellular potentials are applied to the array of axon models in Fig. 8.2, resulting in transmembrane potential increase and activation [61], [99].

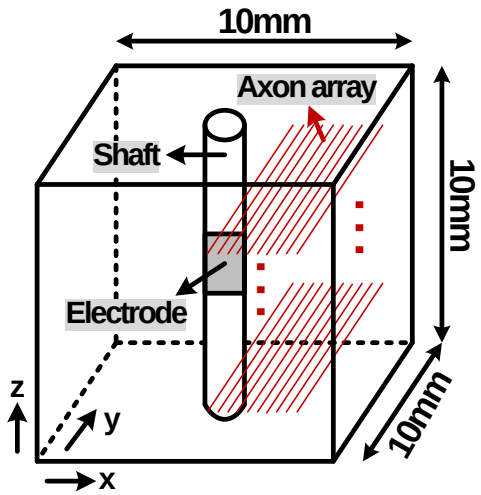


Fig. 8.3. Conceptual tissue model with a stimulation electrode and axon arrays.

Fig. 8.4 shows the 3D tissue model for DBS applications with 10 × 10 × 10 mm^3 volume as shown in Fig. 8.3. The DBS electrode with 1.27 μm diameter and 1.5 μm height was inserted into the tissue along with the electrode shaft. This model utilized a homogeneous isotropic tissue conductivity of 0.3 S/m, while a 0.2 mm thick sheath of encapsulation tissue with a conductivity of 0.15 S/m surrounded the electrode shaft [100]. Fig. 8.5 shows the potential variation in the tissue when 4 mA rectangular current stimulus was applied through the electrode. These time-dependent potential values were

extracted from COMSOL simulation and applied to the outside of the axon model as extracellular potentials through Cadence simulation.

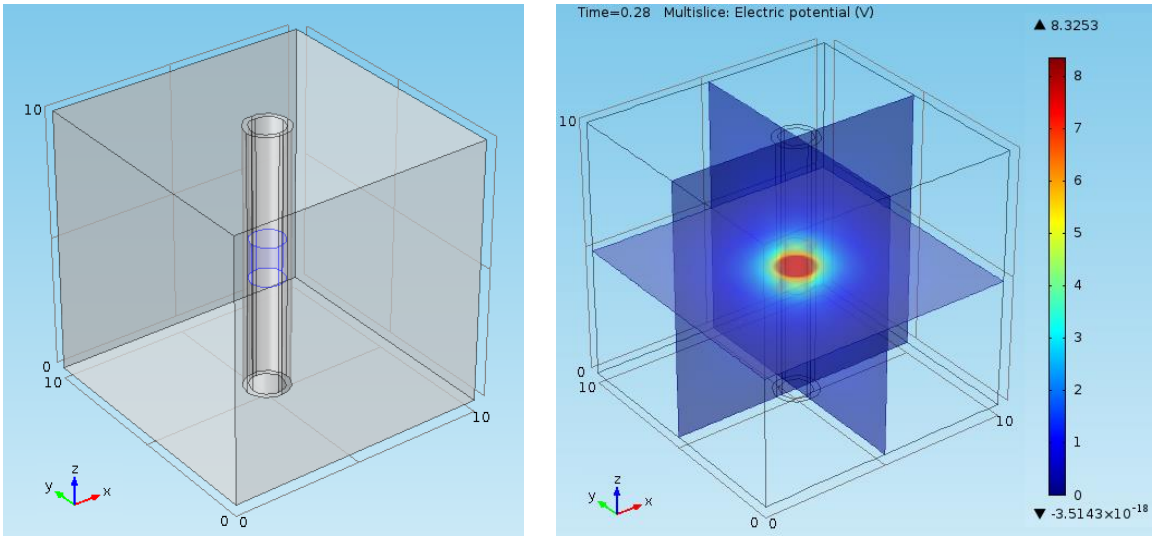
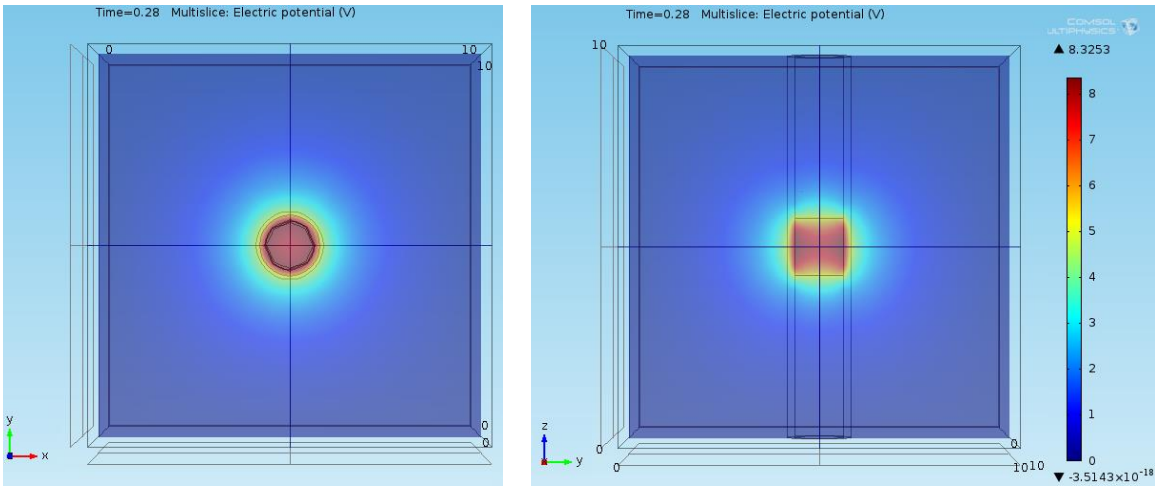


Fig. 8.4. 3D tissue model for DBS application.



(a) Top view (b) Side view

Fig. 8.5. Time-dependent potential variation in the 3D tissue model with (a) top view and (b) side view.

In this simulation, I assumed that a collection of model axons were uniformly distributed in a matrix oriented perpendicular to the electrode shaft as shown in Fig. 8.6 [99]. This orientation of axons was used to identify the spatial extent of activation in the vertical and horizontal directions relative to the electrode shaft. However, localization of activation in axons oriented parallel to the shaft would be ambiguous in the vertical

direction. Therefore, we have assumed that a set of axons, which can be represented as a double-cable array, are placed parallel to the y-axis as shown in Fig. 8.3.

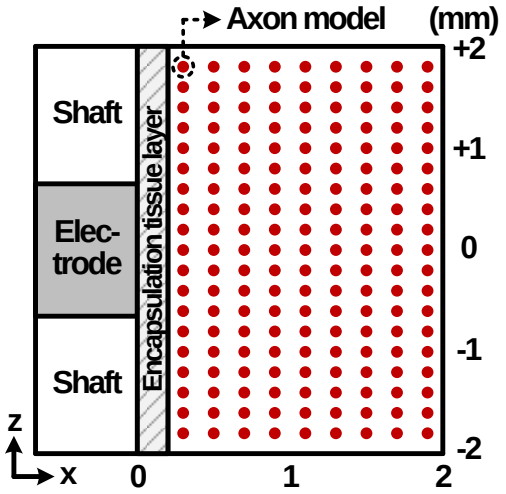
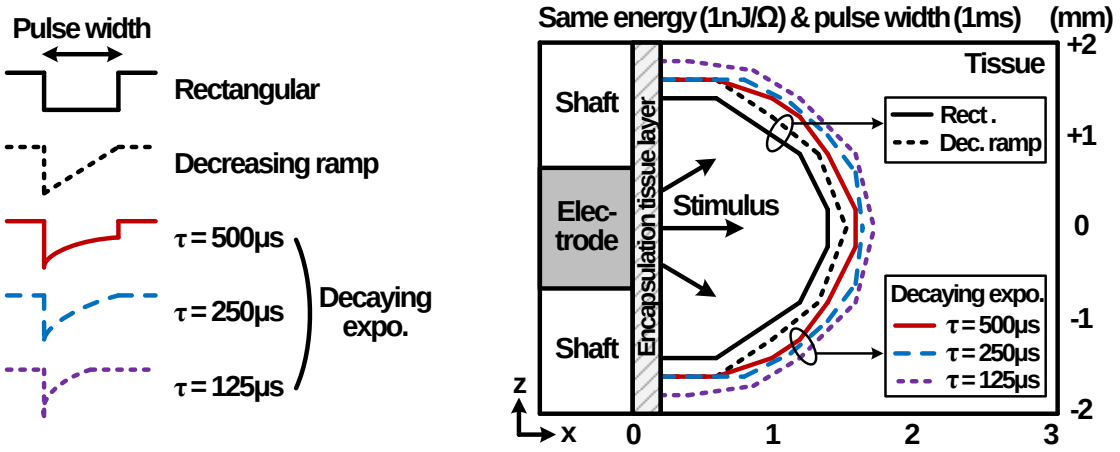


Fig. 8.6. Cross-sectional view of the tissue model with uniformly distributed axons arrays.

8.1.2. Stimulus Efficiency and Waveform Shape

Through the tissue model with the stimulation electrode and axon arrays in chapter 8.1.1, we simulated and analyzed the stimulus efficiency depending on various stimulus waveform shapes. Fig. 8.7 shows how different current stimulus waveforms affect the area of tissue activated when consuming the same amount of stimulus energy for same pulse width. The decaying-exponential stimuli with different time constants (500 μs, 250 μs, and 125 μs) were applied through the electrode along with conventional rectangular and decreasing ramp stimuli as shown in Fig. 8.7a. While the extracellular potentials, which are generated by stimuli in the tissue, stimulate the axon arrays, the neural activation was determined by comparing the increased transmembrane potential of each axon with a predefined threshold level. Fig. 8.7b shows that at the same stimulus energy (= 1 nJ/Ω) and pulse width (= 1 ms), the decaying exponential with smaller time constant can activate larger cross-sectional tissue area than the rectangular and decreasing ramp stimuli.



(a) (b)

Fig. 8.7. (a) Several shapes of stimulus waveforms and (b) area of tissue activated by different stimulus waveform shapes when consuming the same amount of stimulus energy.

Model-simulated results of the stimulus energy, injected charge, and peak stimulus current by the stimulus waveform shapes to activate the same tissue area (= 2.4 mm^2) are shown in Fig. 8.8, while sweeping the stimulus pulse width from 0.1 ms to 1.5 ms. Fig. 8.8a and Fig. 8.8b show that the decaying-exponential stimulus with smaller time constant can activate the same tissue area with smaller stimulus energy and injected charge when the pulse width is larger than 0.4 ms, enabling both energy-efficient and safe stimulation. At 1.5 ms pulse width, the decaying-exponential stimulus requires 40 ~ 70% less stimulus energy and 30 ~ 78% less injected charge in activating the same tissue area compared to other stimulus waveforms, while requiring higher peak amplitude of stimulus current as shown in Fig. 8.8c, which can be accomplished by charging the storage capacitors to higher target voltages in the SCS system. All waveforms show similar stimulus efficiencies with small pulse width (< 0.4 ms). However, since our SCS system can achieve higher stimulator efficiency with the inductive capacitor charger and charge-based stimulation, the overall stimulation efficiency, which is the product of the stimulator efficiency (before electrodes) and the stimulus efficiency (after electrodes), can be still higher than conventional current-regulated stimulator.

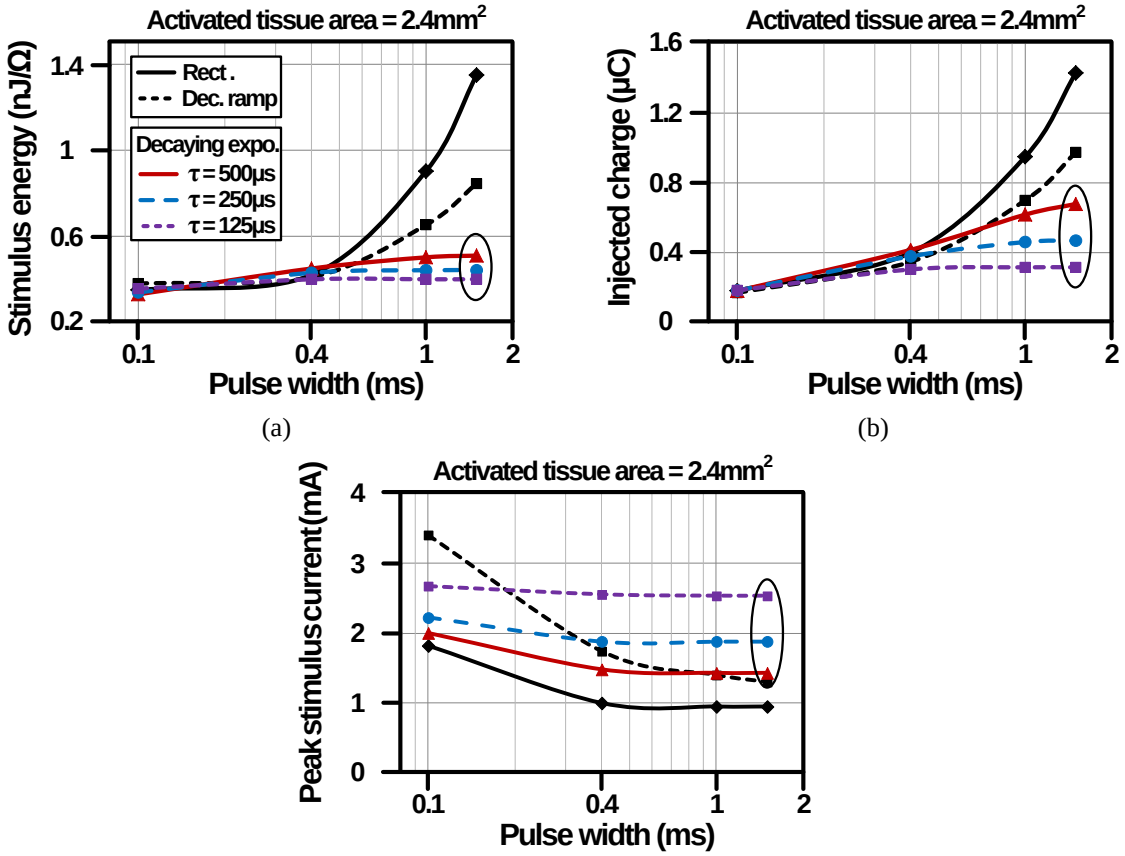


Fig. 8.8. Model-simulated results of (a) stimulus energy, (b) injected charge, and (c) peak stimulus current by stimulus waveform shapes to activate same tissue area of 2.4 mm^2, while sweeping the pulse width.

8.2. *In Vivo* Electrical Stimulation with SCS

To demonstrate the power-efficient charge-based stimulation capability of the SCS system, *in vivo* animal experiments were conducted with an anesthetized cat for brain stimulation. The SCS system provided the decaying-exponential stimulus to the posterior limb of the internal capsule, which is an area of white matter in the brain containing ascending and descending axons, and the evoked neural activities in the contralateral arm muscles generating electromyography (EMG) were recorded through a commercial recording setup. We also measured the EMG signal with conventional voltage stimulation and compared the results with the SCS cases. Fig. 8.9 shows the overall test setup for *in vivo* electrical stimulation with automatic recording and stimulating functions.

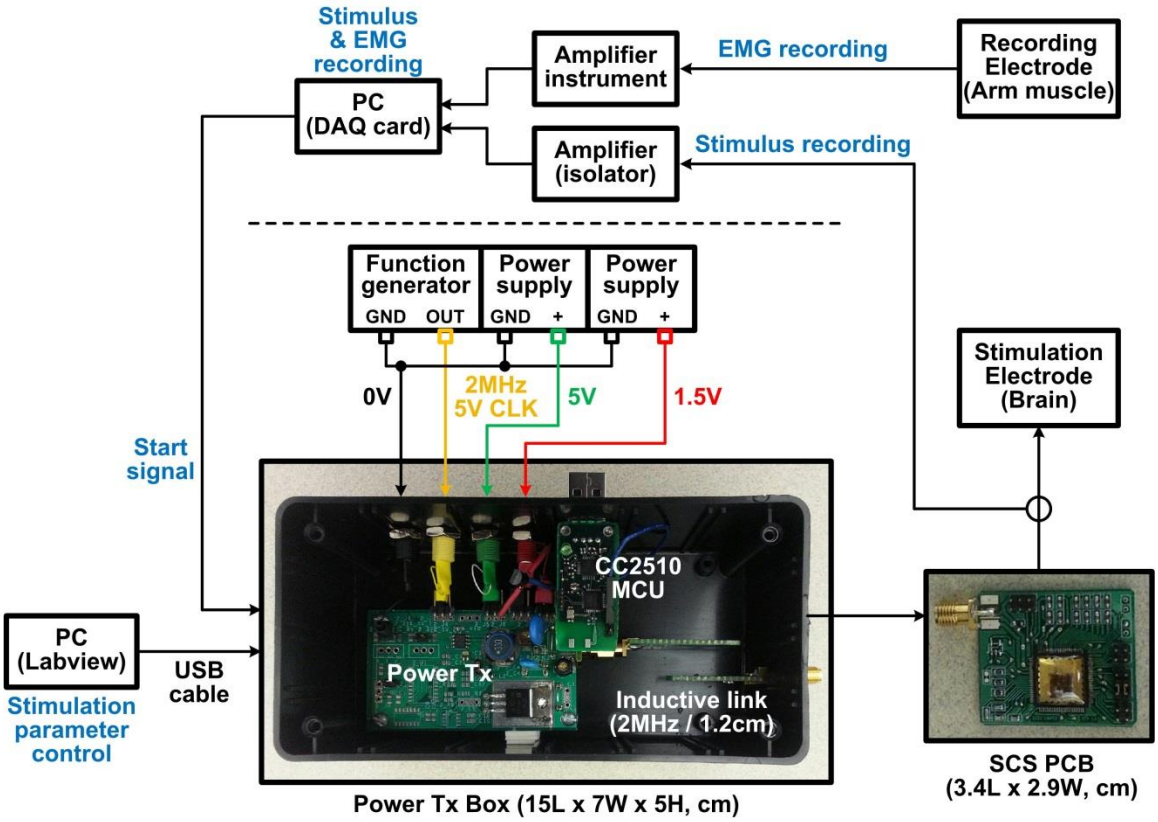
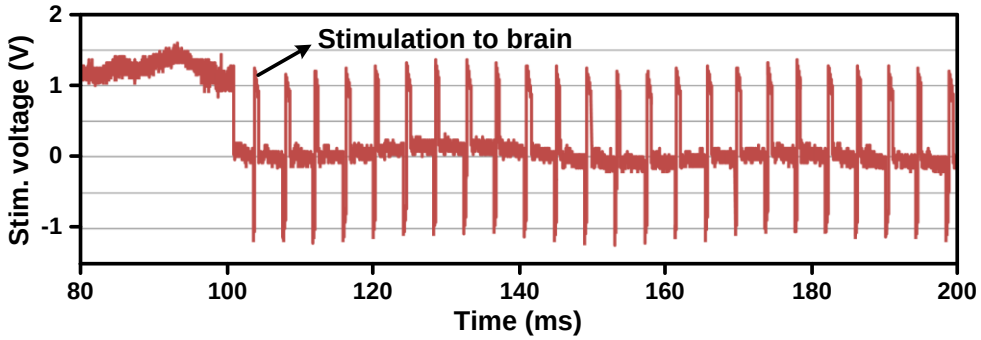


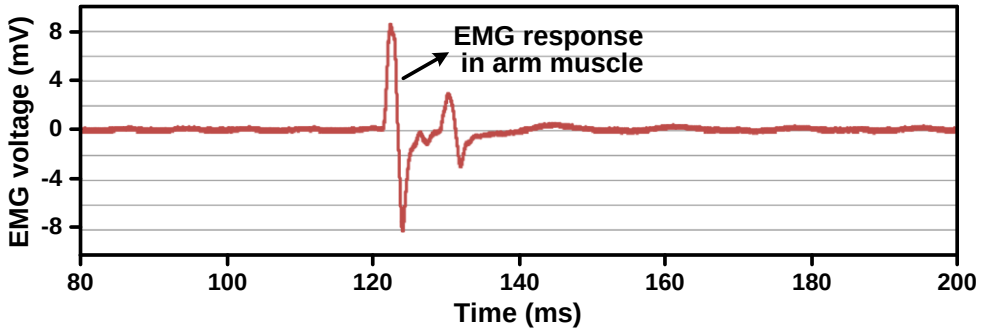
Fig. 8.9. Overall test setup for *in vivo* electrical stimulation with automatic recording and stimulating functions.

In Fig. 8.9, a custom-designed power transmitter (Tx) provides the wireless power to the SCS system though the inductive link at 2 MHz frequency, while the graphic user interface (GUI) with LabVIEW (National Instruments, Austin, Tx) controls the stimulation parameters through forward telemetry. The SCS system, which was populated on 3.4 cm × 2.9 cm PCB, provides the decaying-exponential stimulus to the cat's brain, while the stimulation voltage/current and the EMG voltage from cat's arm muscle were recorded through the amplifier instruments and data acquisition (DAQ) system. For brain stimulation, 30 biphasic pulses at 244 Hz including a 272 μs cathodic pulse followed by a 500 ~ 800 μs charge-balancing anodic pulse were applied, while sweeping the cathodic peak stimulation amplitude in a random manner by charging the negative storage capacitor in SCS between -0.4 V and -1.5 V with 0.1 V resolution. We repeated this stimulation experiment 5 times and calculated the averaged EMG voltage and stimulus energy.

To verify the effects of SCS storage capacitance, we also changed the SCS storage capacitance to 1 μF, 2 μF, 5 μF, and 10μF, with which smaller capacitance results in smaller time constant in the decaying-exponential stimulus. Fig. 8.10 shows the measured biphasic stimulation voltage and its corresponding EMG signal from arm muscle, when -1.2 V peak cathodic-first stimulation pulses were applied to the cat's brain. The EMG response in Fig. 8.10b increased up to 8 mV after ~20 ms delay from the first stimulation pulse.



(a)



(b)

Fig. 8.10. Measured waveforms of (a) the -1.2 V peak biphasic stimulation pulses and (b) the EMG signal from arm muscle.

Fig. 8.11 shows how the decaying-exponential stimulus from SCS affects the stimulus efficiency with *in vivo* EMG results, while comparing to the conventional voltage-regulated stimulation. The recorded EMG signals were rectified and integrated over time, which were averaged through 5 trials. While using higher storage capacitance in SCS results in the decaying-exponential stimulus with larger time constant, the conventional hardwired stimulator provides the rectangular voltage stimulus. In Fig. 8.11a, the EMG signal starts increasing after a certain

threshold level, which depends on stimulus shapes as well as peak stimulus voltage. The conventional voltage-regulated stimulator shows the lowest threshold voltage than the decaying-exponential stimulus from the SCS system, while smaller SCS storage capacitance results in the higher threshold voltage in activating the EMG signals.

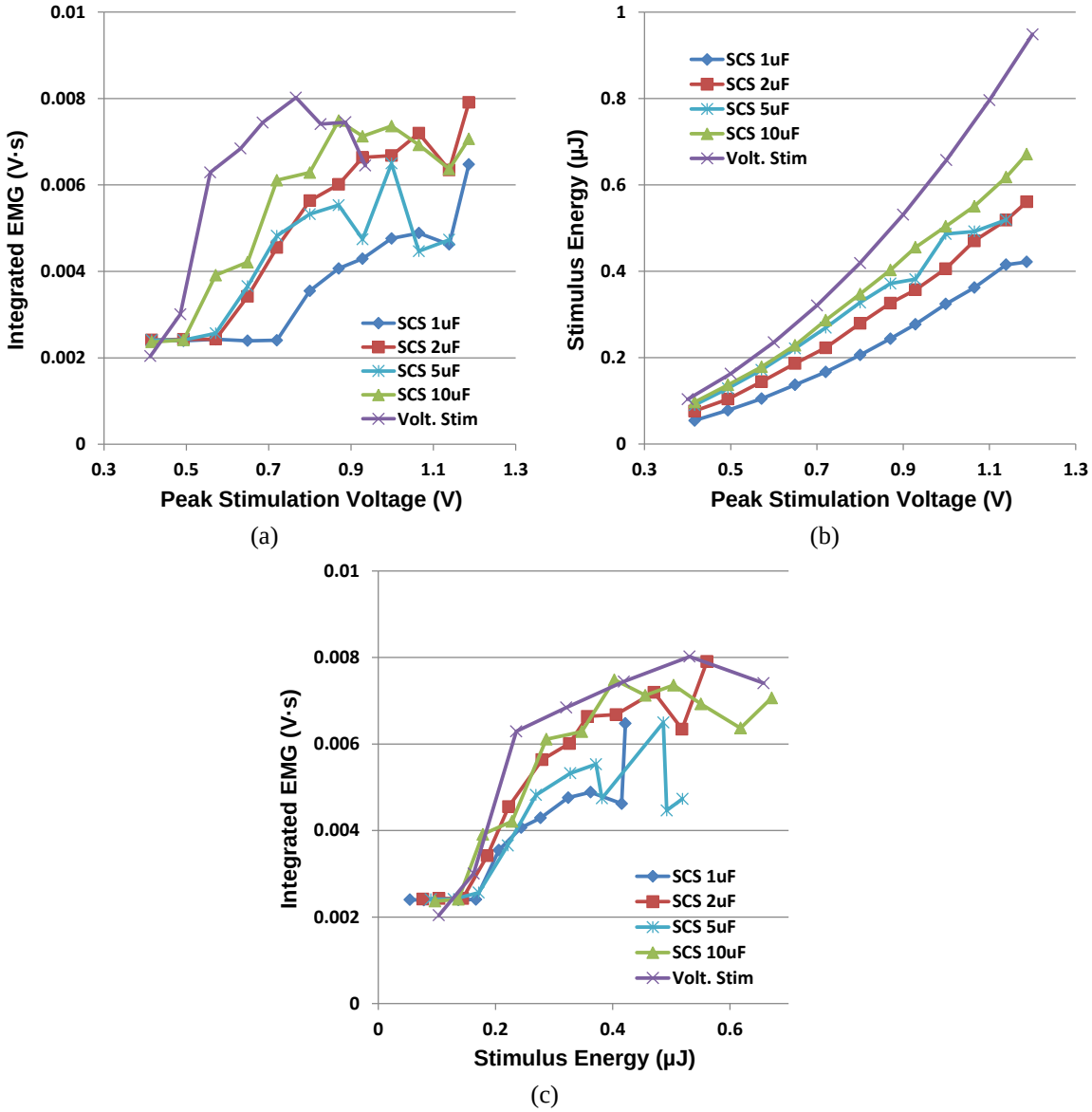


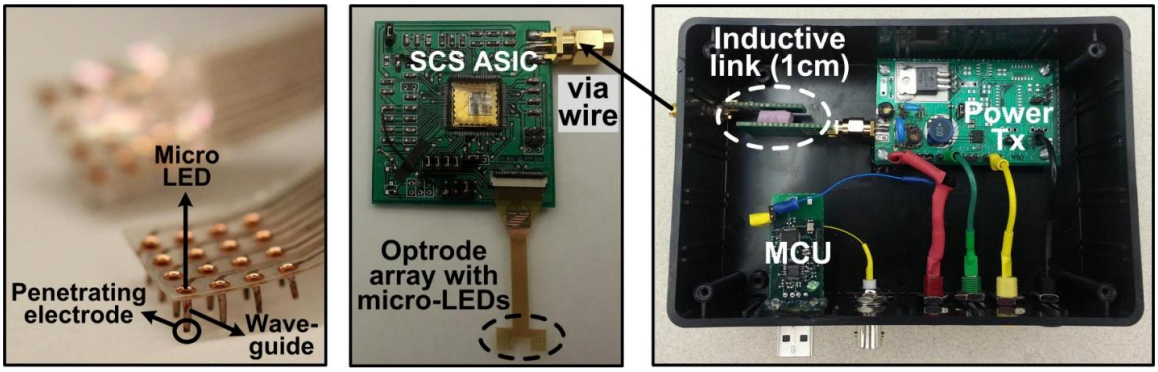
Fig. 8.11. *In vivo* experiment results with SCS. (a) Integrated EMG voltage vs. peak stimulus voltage, (b) Stimulus energy vs. peak stimulus voltage, and (c) integrated EMG voltage vs. stimulus energy graphs.

However, the decaying-exponential stimulus was injecting smaller stimulus energy than the rectangular voltage stimulus when the peak stimulation voltages are the same, as shown in Fig.

8.11b. Therefore, the EMG signals from both rectangular and decaying-exponential stimuli were compared with the injected stimulus energy in Fig. 8.11c. The EMG responses of both stimulus shapes become similar when consuming the same amount of stimulus energy. These results are matched with the model-simulated results in Fig. 8.8a that both rectangular and decaying-exponential stimulus waveforms have similar stimulus efficiencies with small pulse width (< 0.4 ms), while higher stimulator efficiency of the SCS system can further improve the overall efficiency with the decaying-exponential stimulus.

8.3. *In Vivo* Wireless Optogenetics with SCS

In order to verify the capability of power-efficient optogenetics with the SCS system, *in vivo* acute animal experiments were performed with the optrode array and additional recording setup, described in Fig. 7.25. For optogenetics animal experiments, rodent subjects (Sprague-Dawley rats) were viral-transfected with channelrhodopsin-2 (ChR2) to enable light sensitivity. Fig. 8.12 shows the optogenetics test setup including the 3D optrode array with waveguides, the SCS system, and the external power Tx with the inductive link.



(a) (b) (c)

Fig. 8.12. Optogenetics test setup with (a) the 3D optrode array with waveguides, (b) the SCS system, and (c) the external power Tx and inductive link.

Fig. 8.13 shows the *in vivo* experiment setup for optogenetic to the brain (visual cortex, V1) of an anesthetized rat with the SCS system. The inductive link provides the wireless power and data to the SCS system via a twisted pair of connection wires, while

the SCS provides high instantaneous power to the LEDs, generating and delivering sufficient light to the selective target area in the brain through micro-needle waveguides.

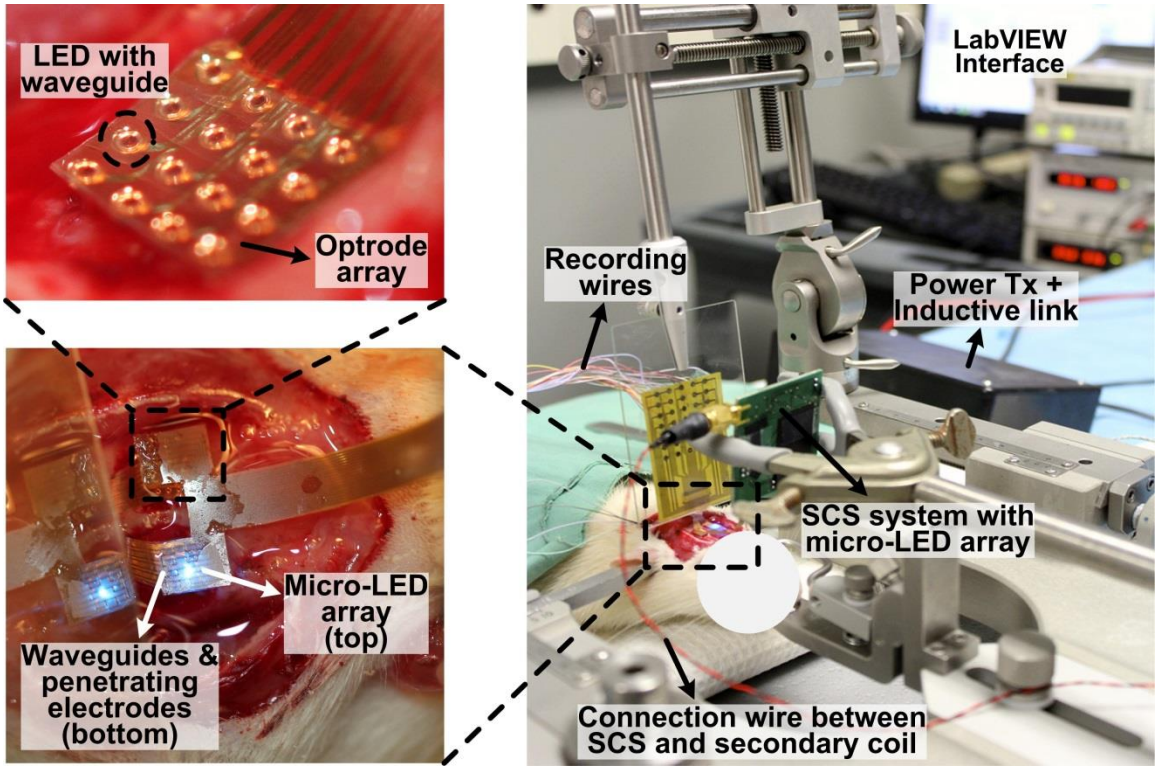


Fig. 8.13. *In vivo* experiment setup for optogenetic experiment on an anesthetized viral-transfected rat with the SCS system.

Fig. 8.14 shows the LED driving voltage, V_{LED}, for optical stimulation with SCS and light-induced *in vivo* local field potential (LFP) results. The LFP below 500 Hz was recorded using an optrode array with waveguides in the brain of the rat when the SCS system drove micro-LEDs with a 0.5 ms pulse train for 100 ms at 1 Hz and V_{LED} = 2.7 V_{peak} and 3.2 V_{peak}, as shown in Fig. 8.14a. While no significant neural modulation was observed with V_{LED} = 2.7 V_{peak}, the higher V_{LED} (= 3.2 V_{peak}) resulted in higher light intensity from micro-LEDs to deliver sufficient irradiance ($\geq$ 1 mW/mm^2) through the micro-needle waveguide for light-evoked neural response in the selective target tissue, leading to larger LFP variations in Fig. 8.14b, which verified the efficacy of optical stimulation via the SCS.

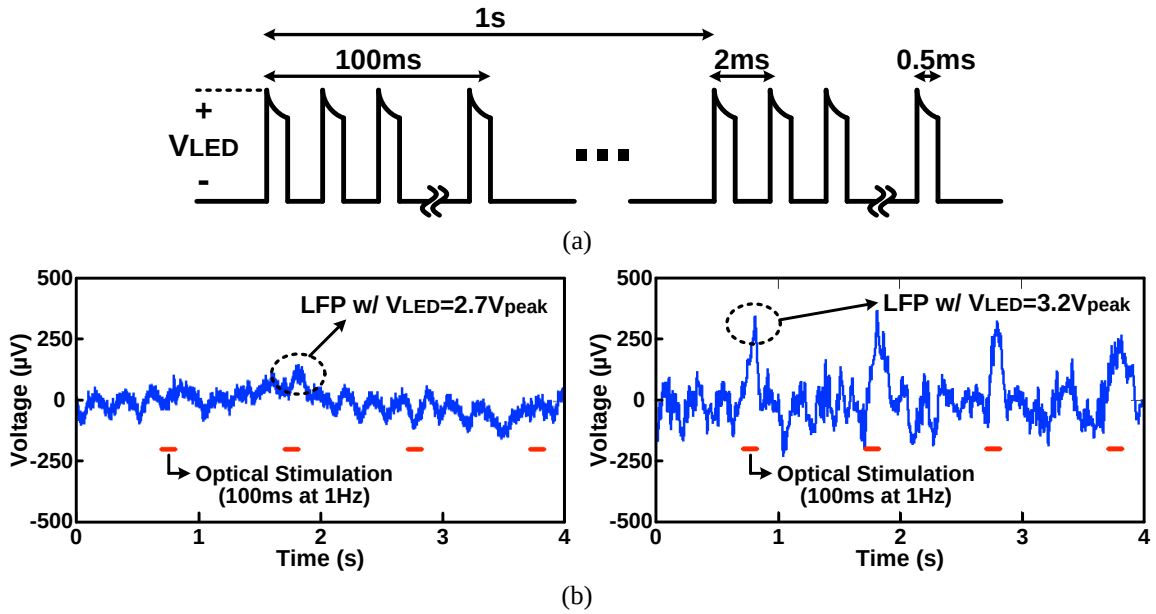


Fig. 8.14. (a) LED driving voltage, V_{LED}, for *in vivo* optogenetics with SCS and (b) light-induced local field potentials (LFP) with V_{LED} = 2.7 V_{peak} and 3.2 V_{peak}.

To visualize neural oscillations generated by the SCS system with optrode arrays clearly, we also measured instantaneous phases of the light-induced LFP with V_{LED} = 2.7 V_{peak} and 3.2 V_{peak} at 1 ~ 25 Hz based on Hilbert Transform as shown in Fig. 8.15. While the SCS system provides 100 ms optical stimulation at 1 Hz, the instantaneous phases of each trial were labeled with different color coding in Fig. 8.15c. In Fig. 8.15a, no phase consistency of neural recording was observed because the micro-LEDs with V_{LED} = 2.7 V_{peak} could not emit sufficient light to the target tissue for stable optogenetics. On the contrary, the light-induced LFP with V_{LED} = 3.2 V_{peak} in Fig. 8.15b showed clear synchronization of instantaneous phases over trials, which was aligned based on the optical stimulation period.

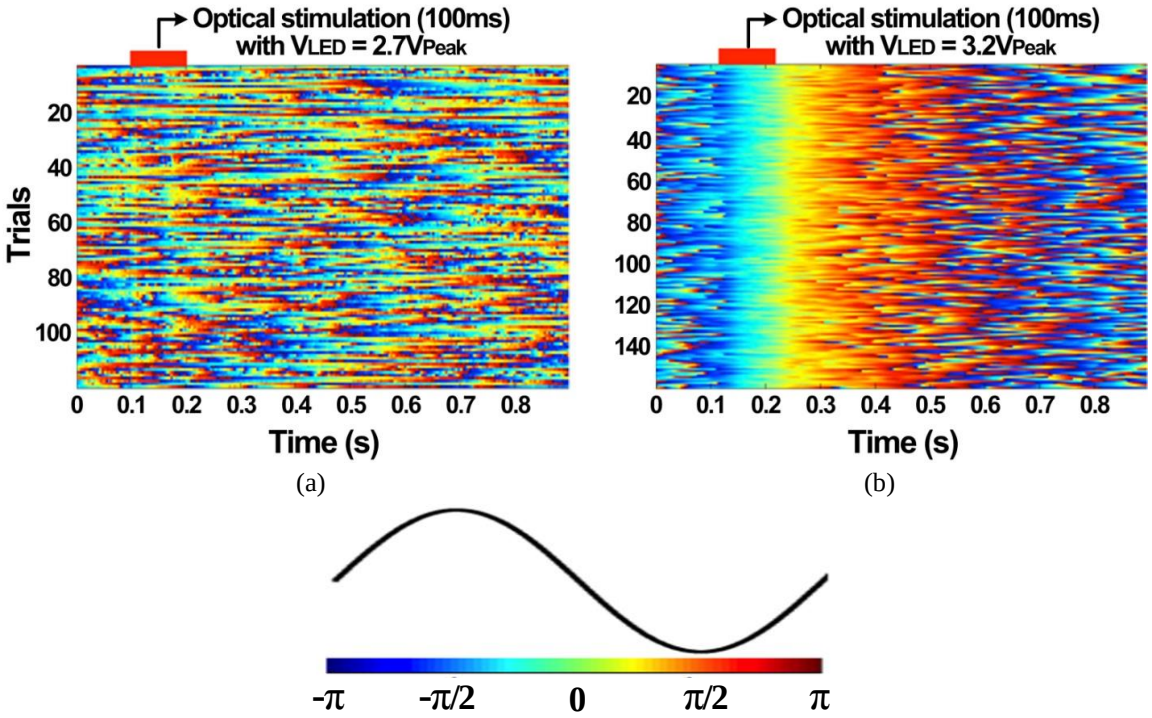


Fig. 8.15. Instantaneous phase of light-evoked LFP at low frequency band (1 ~ 25 Hz) with (a) V_{LED} = 2.7 V_{peak} and (b) V_{LED} = 3.2 V_{peak}. (c) Corresponding color coding.

CHAPTER IX

CONCLUSIONS AND FUTURE WORKS

This dissertation focuses on developing innovative circuit- and system-level techniques for power-efficient wireless neural stimulating systems with inductive power transmission, which has resulted in several journal and conference publications [65], [69], [101]-[111]. The proposed AC-to-DC converters such as an active rectifier, an active voltage doubler, and an adaptive reconfigurable voltage doubler/rectifier (VD/REC) significantly improve the power conversion efficiency (PCE) and extend the inductive power transmission range, while the power-management circuits including these AC-to-DC converters can be utilized for not only wireless neural stimulating systems but also various inductive powered applications. The adaptive wireless neural stimulating system with closed-loop supply control enables safe and accurate current-based stimulation, while adopting adaptive supply control to automatically adjust stimulation compliance voltages by detecting stimulation site potentials, improving the stimulator efficiency. The proposed switched-capacitor stimulating (SCS) system takes advantage of both high efficiency and safety by utilizing an inductive capacitor charger and charge-based stimulation, leading to power-efficient electrical and optical stimulation. This chapter summarizes the results and scientific contributions of this dissertation, followed by future works.

9.1. Conclusions

9.1.1. Power-management Circuits with Inductive Power Transmission

An integrated power-efficient full-wave active rectifier equipped with offset-controlled high speed comparators was presented for inductively powered applications, such as RFID and IMD. The main switches in this rectifier are driven by a pair of comparators, which keep them closed precisely, while compensating for both turn-on and

turn-off propagation delays of the comparators by a pair of programmable offsets. As a result, the rectifier conducts for the maximum possible period of time and delivers maximum forward current to the load, while minimizing the back current. In addition, the sizes of the rectifying transistors were optimized for minimizing their R_{on} and switching losses at the rectifier operating frequency. We have reported the highest measured PCE of 80.2% with 3.12 V DC output across a 500 Ω load from a 3.8 V AC input at 13.56 MHz.

While comparator-based active rectifiers are considered the most promising solutions to achieve not only high PCE but also low dropout voltage in inductive power transmission, these active rectifiers need peak input voltage that should always be higher than the desired output voltage. This will limit the operation range and safe voltages of most inductively powered devices, such as IMDs and RFID tags, which tend to have weakly coupled links. In order to overcome this limitation, we have also developed a fully integrated power-efficient active voltage doubler with triple offset-controlled functions, which can offer high PCE and low dropout voltage comparable to active rectifiers, while increasing the output voltage, V_{OUT}, well above the peak input voltage, $V_{IN,Peak}$. Three different offset control functions, built in the comparators, compensate for their turn-on and turn-off delays to maximize forward current to the load, while ensuring the reliable turn-off operation. In addition, a novel startup circuit has been added to the voltage doubler to guarantee its reliable initial operation as a passive voltage doubler when V_{OUT} = 0 V. The relationship between the active voltage doubler PCE, dropout voltage, and several power loss factors has also been analyzed to provide designers with better insight towards maximizing the PCE. With 1.46 V peak AC input at 13.56 MHz, the active voltage doubler provides 2.4 V DC output across a 1 kΩ load, achieving the highest PCE = 79% ever reported at this frequency.

Inductive power transmission across the skin is considered the most promising solution for providing sufficient power to IMDs without suffering from size and power constraints of implanted batteries. However, large variations in the received voltage

across the secondary coil, which mainly result from coil misalignments or loading variations, can lead to insufficient supply voltage for the IMD. In order to overcome this limitation, we have developed a power-efficient adaptive reconfigurable active voltage doubler/rectifier, which can automatically change its operating mode to operate either as a voltage doubler or a rectifier, depending on which one is more suitable for generating the desired output voltage at the highest possible PCE, enabling robust power transmission across the inductive link over an extended range. The presented VD/REC has been equipped with active diodes, in which high speed comparators synchronously control MOS switches at proper times thanks to their turn-on and turn-off offset functions, achieving high PCE and low dropout voltage. Measured results while sweeping the coils relative distance and orientation clearly verify that using the VD/REC extends the inductive power transmission range in both air and muscle environments. In an exemplar setup, VD/REC extended the power transmission range by 33% (from 6 cm to 8 cm) in relative coil distance and 41.5% (from 53° to 75°) in relative coil orientation compared to using the rectifier alone. While providing 3.1 V DC output across a 500 Ω load from 2.15 V (VD) and 3.7 V (REC) peak AC inputs at 13.56 MHz, VD/REC achieved measured PCE of 70% and 77%, respectively.

Moreover, the proposed power-management circuits including the aforementioned active AC-to-DC converters were adopted in several wireless biomedical microsystems developed in GT-bionics lab, such as a wireless integrated neural-recording system (WINeR) in [65] and an intraoral tongue-drive system (iTDS) in [69], to provide sufficient wireless power through the inductive link while achieving high PCE. The power-management circuits in these biomedical microsystems have been equipped with additional features such as low-dropout regulators (LDO), forward and back data telemetry, an overvoltage protection circuit, and battery charging and monitoring circuits.

9.1.2. Wireless Neural stimulating System with Adaptive Supply Control

Current-controlled stimulators (CCS) have been widely used in implantable electrical stimulators because of their precise current control and safe operation. However, CCS suffers from low power efficiency, which mainly results from the large voltage drop across the output current sources, especially when the necessary stimulation voltage is much smaller than the supply voltage. In order to improve the CCS power efficiency, we have proposed an internal closed loop system for adaptive control of the stimulator supply voltage slightly above the peak of the stimulation voltage.

This mechanism significantly reduces the power loss in the CCS current sources, helping the CCS achieve high stimulation efficiency regardless of the stimulation voltage levels, while taking advantage of its safety features, completed by adopting the active charge balancing mechanism to neutralize the residual charge. The adaptive supply voltage has been generated directly from the inductive link using the proposed adaptive rectifier, which has high measured AC-DC PCE for the multilevel DC output thanks to the phase control feedback. The wireless stimulating system also includes a voltage readout channel to close the on-chip control feedback loop as well as the amplitude-shift-keying (ASK) demodulation block for forward data telemetry.

A 4-ch wireless stimulating system prototype was fabricated in a 0.5-μm 3M2P standard CMOS process, occupying 2.25 mm^2. With 5 V peak AC input at 2 MHz, the adaptive rectifier provides an adjustable DC output between 2.5 V and 4.6 V at 2.8 mA loading, resulting in measured PCE of 72 ~ 87%. The adaptive supply control increases the stimulation efficiency up to 30% higher than a fixed supply voltage to 58 ~ 68%. Bench-top and *in vitro* measurement results of a fabricated prototype verified that the proposed inductively powered wireless stimulating system with adaptive supply control was fully functional and improved the overall power efficiency of wireless stimulators for applications such as DBS and cochlear implants.

9.1.3. Power-efficient Switched-capacitor Stimulating (SCS) System

We have proposed a wireless switched-capacitor stimulating (SCS) system, which takes advantage of high efficiency, high driving capability, and safety, for both electrical and optical deep brain stimulation. The proposed SCS system efficiently charges storage capacitor pairs directly from the inductive link through a dual-control inductive capacitor charger, while connecting negative and positive capacitors alternately to the tissue for charge-based stimulation, improving stimulator efficiency (before electrodes). A charge monitoring circuit measures the amount of charge injected and withdrawn, and adaptively changes the stimulus pulse width to neutralize the residual charge in the tissue, ensuring charge balancing. The SCS system also utilizes on-off-keying pulse-position-modulated (OOK-PPM) forward telemetry and load-shift-keying (LSK) back telemetry for robust bi-directional wireless data communication, while an on-chip timing controller and power management unit enable the fully integrated wireless SCS system-on-a-chip.

Tissue modeling and stimulus efficiency analysis have proven that a decaying-exponential stimulus shape, which can be generated by SCS without consuming additional power, requires smaller stimulus energy and injected charge to activate the same tissue area compared to conventional rectangular and ramp stimuli, improving stimulus efficiency (after electrodes). A 4-ch wireless SCS system in 0.35 μm CMOS process achieved high stimulator efficiency of 80.4% with ±2 V capacitor pairs, while the decaying-exponential stimulus requires smaller stimulus energy (40~70% less) and injected charge (30~78% less) to activate the same tissue area than other stimuli when the pulse width is 1.5 ms. With smaller pulse width (< 0.4 ms), all stimulus waveforms show similar stimulus efficiencies, while our SCS system can achieve higher stimulator efficiency than the conventional CCS. The SCS system has also been utilized for power-efficient wireless optogenetics by periodically discharging capacitors into high-current micro-LED arrays. *In vivo* results verify the efficacy of the SCS for both electrical and optical stimulation.

9.2. Future Works

While the SCS system has been utilized for *in vivo* animal experiments for both electrical and optical stimulation with anesthetized animal subjects in chapter 8, the SCS system will be also utilized for freely moving animal experiments to prove its stimulating function in practical *in vivo* condition for behavioral responses. The SCS system receives wireless power through the weakly coupled inductive link that can be misaligned due to animal's movements, resulting in variation of transferred power. To address this issue, the SCS system adopted the closed-loop power control technique with LSK back telemetry capability, which should be further tested with a custom-designed external power Tx. In freely moving animal experiments, the animal subject will wear a jacket with a backpack, which includes the power Tx with RFID functions, the external battery, and the primary (transmitter) coil, while the secondary (receiver) coil and the SCS chip (headstage) will be placed on the back and head of the animal subject, respectively, providing the stimulation pulses to either electrodes or micro-LEDs in the brain, as shown in Fig. 9.1.

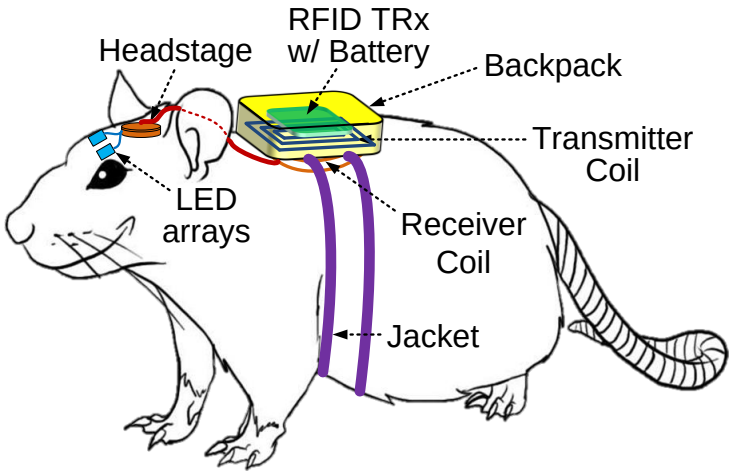


Fig. 9.1. Freely moving animal experiment setup with the backpack for wireless powering.

In addition, the wireless SCS chip will be used for the system-level integration of interface IC with an opto-electro array on a single flexible polymer platform, suitable for

chronic implantation in the brain of small freely behaving animals. The integrated SCS system will be capable of providing both electrical and optical stimuli efficiently, while additional neural-recording setup will simultaneously record and monitor multichannel neural signals in real time through the wireless interface. The wireless SCS system will be populated on the flexible-substrate PCB using the flip-chip technique to minimize the implant size (< 2cc), and the power receiving coil will be fabricated on the same flexible-substrate PCB, which will be folded to form the compact chronic implant for closed-loop neuromodulation. Innovative packaging strategies to minimize bioreactivity, biofouling, and mechanical mismatches between the devices and tissue will be also developed by our collaborators to maintain the long-term reliability and stability of the system.

Regarding the decaying-exponential stimulus waveforms of the SCS system, its stimulation effects should be further measured through several additional *in vivo* animal experiments. These results will be compared with other conventional voltage- or current-regulated stimulation as well as previous animal experiment data to ensure reliable and trustful *in vivo* results, while verifying the energy-efficient stimulus waveform in the SCS system.

In the distributed stimulating system, we have already fabricated the improved distributed stimulator chip in TSMC 0.35-μm standard CMOS process. The fully on-chip distributed stimulator IC module includes a power-management block, current stimulator, and forward/back telemetry, occupying only 2.4 mm × 1.1 mm, which can be placed near each DBS electrode for distributed stimulating function. The distributed stimulator IC should be fully characterized, and the overall distributed stimulating system prototype, in which several IC modules are connected in series through only two input wires, will be verified for multichannel DBS application.

APPENDIX

PCE ANALYSIS OF THE ACTIVE RECTIFIER

In this section we derive (2.1) and (2.3) for PCE analysis using simplified rectifier waveforms, shown in Fig. A.1. D is the rectifier switching duty cycle, D_{charge} is the charging duty cycle, $T = 1/2f_c$ is the period of the full-wave rectified signal, and T_{PHL} and T_{PLH} are the delays in high-to-low and low-to-high transitions of the comparator output (V_{OUT}), respectively.

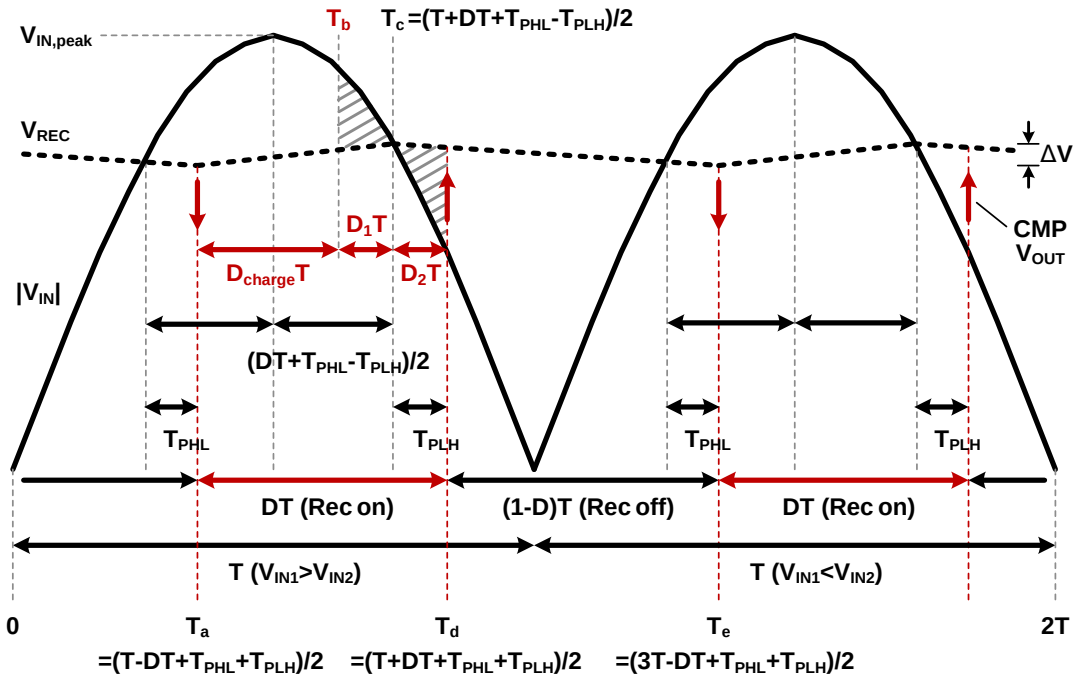


Fig. A.1. Simplified voltage waveforms of the active rectifier used in the PCE theoretical analysis. To simplify the equations, we have assumed $\Delta V \rightarrow 0$ V.

In this model, we assume: 1) V_{IN} is sinusoidal, 2) R_L is constant, 3) C_L is large enough to maintain V_{REC} almost constant despite the rectifier operation, and 4) the rising and falling times of the comparator output are negligible compared to T (or they have been included in T_{PHL} and T_{PLH}). The rectifier turns on (i.e. conducts) from T_a to $T_d = DT$ and turns off from T_d to $T_e = T - DT$. The assumption is that the additional charge that is stored in C_L during DT maintains V_{REC} constant while the rectifier is supplying R_L for the

entire period of T. Therefore,

$$\int_{T_a}^{T_d} I_{in}(t)\,dt = \int_{T_a}^{T_d} \left(\frac{V_{IN}(t) - V_{REC}}{R_{onp} + R_{onn}} \right) dt$$
$$= \int_{T_a}^{T_e} \left(\frac{V_{REC}}{R_L} \right) dt = \frac{V_{REC}}{R_L} T \qquad \text{(A.1)}$$

where $T_a = (T\text{-}DT\text{+}T_{PHL}\text{+}T_{PLH})/2$, $T_d = (T\text{+}DT\text{+}T_{PHL}\text{+}T_{PLH})/2$, and $T_e = (3T\text{-}DT\text{+}T_{PHL}\text{+}T_{PLH})/2$ are indicated on Fig. A.1. The sinusoidal input voltage, V_{IN}, can be expressed as,

$$V_{IN}(t) = V_{IN,peak} \sin\left(\frac{\pi}{T} t \right)$$
$$= \frac{V_{REC}}{\sin\left(\left(T_a - T_{PHL} \right) \frac{\pi}{T} \right)} \sin\left(\frac{\pi}{T} t \right) \qquad \text{(A.2)}$$

Using (A.2) in (A.1), $R_{onp} + R_{onn}$ can be expressed as a function of D,

$$R_{onp} + R_{onn} = R_L \left(\frac{\frac{1}{\pi}\left(\cos\left(T_a \frac{\pi}{T} \right) - \cos\left(T_d \frac{\pi}{T} \right) \right)}{\sin\left(\left(T_a - T_{PHL} \right) \frac{\pi}{T} \right)} - D \right) \qquad \text{(A.3)}$$

If $T_{PLH} = 0$, D_{charge} would be the same as D because the rectifier only supplies $R_L C_L$ during its conducting period. However, with $T_{PLH} > 0$, the back current can discharge C_L when $V_{REC} > |V_{IN}|$. In Fig. A.1, the back current from T_c to T_d (D_2T) discharges C_L as much as the forward current from T_b to T_c (D_1T) charges C_L. Therefore, D_{charge} can be derived as a function of D by obtaining T_b,

$$\begin{cases} I_{in} = I_{C_L,charge} + I_{R_L} & T_b < t < T_c \\ I_{in} = I_{C_L,discharge} + I_{R_L} & T_c < t < T_d \end{cases} \qquad \text{(A.4)}$$

$$\int_{T_b}^{T_c} I_{C_L,charge}(t)\,dt + \int_{T_c}^{T_d} I_{C_L,discharge}(t)\,dt$$
$$= \int_{T_b}^{T_d} \left(\frac{V_{IN}(t) - V_{REC}}{R_{onp} + R_{onn}} - \frac{V_{REC}}{R_L} \right) dt = 0 \tag{A.5}$$

By solving (A.1)-(A.5) for T_b using MATLAB, D_{charge} can be expressed as,

$$D_{charge} = D - \left(\frac{T_d - T_b}{T} \right) \tag{A.6}$$

Note that even though the input current from T_b to T_d does not affect V_{REC}, R_{on} power losses still occur during this period (D_1T+D_2T). Therefore, the R_{on} loss term with D_{eff} in (2.1) can be represented as,

$$P_{Loss,R_{onp}} + P_{Loss,R_{onn}} = \left(\frac{V_{REC}}{R_L D_{eff}} \right)^2 D_{eff} \left(R_{onp} + R_{onn} \right)$$
$$= \left(\left(\frac{V_{REC}}{R_L D_{charge}} \right)^2 D_{charge} + \left(\frac{1}{D_1 T} \int_{T_b}^{T_c} I_{in}(t)\,dt \right)^2 D_1 \right.$$
$$\left. + \left(\frac{1}{D_2 T} \int_{T_c}^{T_d} I_{in}(t)\,dt \right)^2 D_2 \right) \left(R_{onp} + R_{onn} \right) \tag{A.7}$$

where the first, second, and third terms of the right-hand side equation correspond to the R_{on} loss during $D_{charge}T$, D_1T, and D_2T, respectively. If T_{PLH} = 0, the second and third terms will be eliminated because $T_b = T_c = T_d$. Therefore, using (A.1)-(A.7), the R_{on} loss in (2.1) can be expressed as a function of D.

$R_{onp} + R_{onn}$ can also be represented as a function of $W_p = W_n$,

$$R_{onp} + R_{onn} = \frac{1}{W_p} \left(\frac{L_{min}}{k_p (V_{REC} - |V_{ThP}|)} + \frac{L_{min}}{k_n (V_{REC} - V_{ThN})} \right) \tag{A.8}$$

where L_{min} is the length of the PMOS and NMOS transistors. By substituting W_p with (A.8), the switching loss term, $P_{Loss,Cgp}$, in (2.1) can be expressed as a function of D,

$$P_{Loss,C_{gp}} = W_p C_{gp}^{*} V_{REC}{}^2 2 f_c = C_{gp}^{*} V_{REC}{}^2 2 f_c \times \frac{1}{R_{onp} + R_{onn}} \left(\frac{L_{min}}{k_p (V_{REC} - |V_{ThP}|)} + \frac{L_{min}}{k_n (V_{REC} - V_{ThN})} \right) \quad \text{(A.9)}$$

Therefore, by substituting (A.7) and (A.9) in (2.1) and differentiating it with respect to D, we can obtain the optimized D for minimum power loss inside the rectifier. Using the optimal D, the optimal W_p can be derived from (A.3) and (A.8), and the maximum PCE can be calculated from (2.3) by minimizing the power loss in (2.1).

PCE ANALYSIS OF THE ACTIVE VOLTAGE DOUBLER

In this section, we calculate the PCE in (2.5) and V_{Drop} in (2.4) using simplified voltage doubler waveforms shown in Fig. A.2. In this analysis, D is the voltage doubler operating duty cycle, V_{Cin} is the voltage across C_{IN}, and $T = 1/f_c$ is the period of one operating cycle.

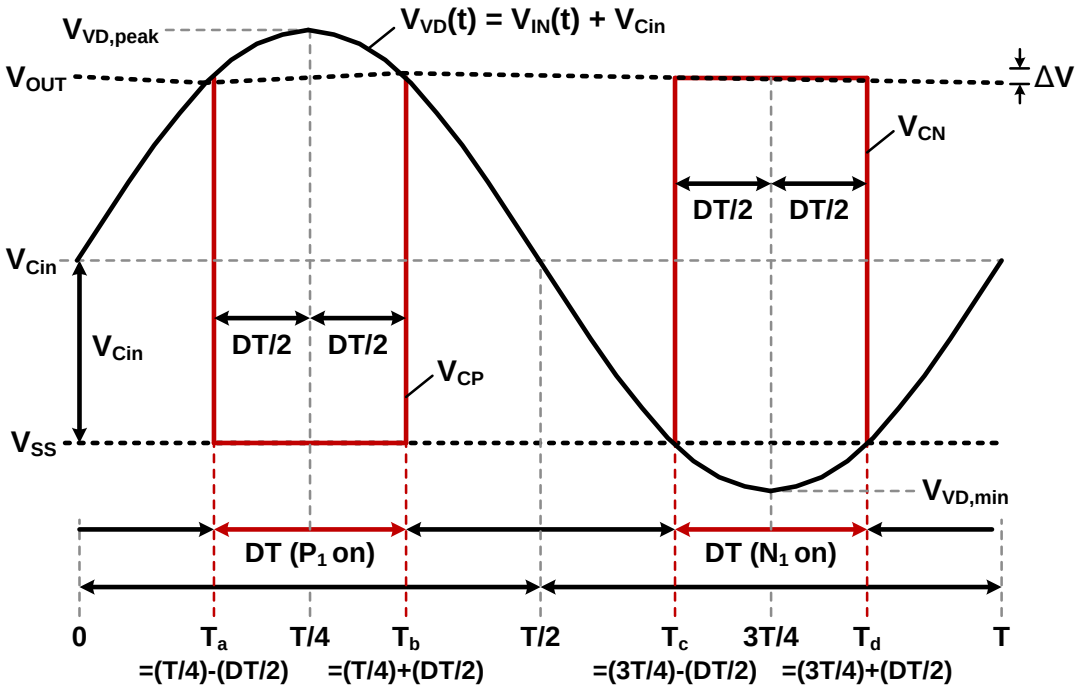


Fig. A.2. Simplified voltage waveforms of the active voltage doubler for the theoretical PCE analysis.

In this simplified model, we assume: 1) $V_{IN}(t)$ is sinusoidal, 2) C_L and C_{IN} are large enough to maintain V_{OUT} and V_{Cin} almost constant during $T/2$, i.e. $\Delta V \approx 0$ V. 3) comparators turn on and off their pass transistors, P_1 and N_1, at ideal times and their outputs, V_{CP} and V_{CN}, have negligible rising and falling times, and 4) $V_{VD,peak} - V_{OUT} = V_{SS} - V_{VD,min}$, therefore, V_{Cin} can be expressed as $V_{OUT}/2$.

For this analysis, we also used the optimal size ratio of P_1 and N_1 in [64] which leads to minimum $R_{onp} + R_{onn}$ in a given area,

$$\left(\frac{W_p}{W_n}\right)_{opt} = \sqrt{\frac{\mu_n C_{ox}(V_{OUT} - V_{Thn})}{\mu_p C_{ox}(V_{OUT} - |V_{Thp}|)}}. \quad (A.10)$$

While (2.6) and (2.7) can be solved directly by knowing circuit parameters, D needs to be derived to obtain $P_{Tr.Ron}$ in (2.8),

$$D = \frac{T_b - T_a}{T} = \frac{T_d - T_c}{T} \quad (A.11)$$

$$T_a = \frac{T}{4} - \frac{DT}{2}, \qquad T_b = \frac{T}{4} + \frac{DT}{2},$$

$$T_c = \frac{3T}{4} - \frac{DT}{2}, \qquad T_d = \frac{3T}{4} + \frac{DT}{2}. \quad (A.12)$$

The charging current flowing through pass transistors, P_1 and N_1, needs to be the same as the total output and dissipated currents of the voltage doubler. Therefore,

$$\int_{T_a}^{T_b} I_p dt = \int_{T_c}^{T_d} I_n dt = \int_0^T \left(I_{Load} + I_{CMP} + I_{Tr,sw}\right) dt \quad (A.13)$$

$$\int_{T_a}^{T_b} I_p dt = \int_{\frac{T}{4}-\frac{DT}{2}}^{\frac{T}{4}+\frac{DT}{2}} \frac{V_{VD}(t) - V_{OUT}}{R_{onp}} dt$$

$$= \left(\frac{V_{OUT}}{R_L} + \frac{P_{CMP}}{V_{OUT}} + \frac{P_{Tr,sw}}{V_{OUT}}\right) T. \quad (A.14)$$

In (A.14), $V_{VD}(t)$ can be written as,

$$V_{VD}(t) = V_{IN}(t) + V_{Cin} = V_{IN}(t) + \frac{V_{OUT}}{2}$$

$$= V_{IN,peak} \sin\left(\frac{2\pi}{T}t\right) + \frac{V_{OUT}}{2}$$

$$= \frac{\frac{V_{OUT}}{2}}{\sin\left(\frac{2\pi}{T}T_a\right)} \sin\left(\frac{2\pi}{T}t\right) + \frac{V_{OUT}}{2}. \quad (A.15)$$

By substituting (A.15) in (A.14), D can be obtained with given values of R_{onp}, R_L, and V_{OUT} from,

$$R_{onp}\left(\frac{1}{R_L} + \frac{P_{CMP} + P_{Tr,sw}}{{V_{OUT}}^2}\right) = \left(\frac{\cos\left(\left(\frac{1}{2} - D\right)\pi\right) - \cos\left(\left(\frac{1}{2} + D\right)\pi\right)}{4\pi \sin\left(\left(\frac{1}{2} - D\right)\pi\right)} - \frac{D}{2}\right) \quad (A.16)$$

where P_{CMP} and $P_{Tr,sw}$ can be approximated from the simulation results and (2.7), respectively. Then, we can solve $P_{Tr.Ron}$ in (2.8) using D from (A.16), and the PCE can be calculated by substituting (2.6) - (2.8) in (2.5). In addition, using MATLAB we can easily try various R_{onp} values (e.g. by changing W_p) and find the optimal size of the pass transistors, which results in minimum power loss and maximize the PCE. V_{Drop} can also be estimated by obtaining $V_{IN,peak}$ from (A.15) and substituting it in (2.4).

REFERENCES

[1] B. S. Wilson and M. F. Dorman, "Cochlear implants: A remarkable past and a brilliant future," *Hearing Res*., vol. 242, no. 1-2, pp. 3-21, Aug. 2008.

[2] D. Shire, S. Kelly, J. Chen, P. Doyle, M. Gingerich, S. Cogan, W. Drohan, O. Mendoza, L. Theogarajan, J. Wyatt, and J. Rizzo, "Development and implantation of a minimally invasive wireless subretinal neurostimulator," *IEEE Trans. Biomed. Eng*., vol. 56, no. 10, pp. 2502-2511, Oct. 2009.

[3] M. Ortmanns, M. Gehrke, and H. Tiedtke, "A 232-channell epiretinal stimulator ASIC," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2946-2956, Dec. 2007.

[4] L. D. Cruz, B. F. Coley, J. Dorn, F. Merlini, E. Filley, P. Christopher, F. K. Chen, V. Wuyyuru, J. Sahel, P. Stanga, M. Humayun, R. J. Greenburg, and G. Dngnelie, "The Argus II epiretinal prosthesis system allows letter and word reading and long-term function in patients with profound vision loss," *Br. J. Ophthalmol*. Feb. 2013.

[5] A. V. Nurmikko, J. P. Donoghue, L. R. Hochberg, W. R. Patterson, Y.-K. Song, C. W. Bull, D. A. Borton, F. Laiwalla, S. Park, Y. Ming, and J. Aceros, "Listening to brain microcircuits for interfacing with external world-progress in wireless implantable microelectronic neuro- engineering devices," *Proc. IEEE*, vol. 98, pp. 375-388, Mar. 2010.

[6] M. Ghovanloo, "Integrated circuits for neural interfacing: Neural stimulation," in *VLSI Circuits for Biomedical Applications*, K. Iniewski, Ed. Norwood, MA: Artech House, 2008.

[7] M. Rasouli and L. S. Phee, "Energy sources and their development for application in medical devices," *Expert review of Medical Devices*, vol. 7, no. 5, pp. 693-709, 2010.

[8] S.A.P. Haddad, R.P.M. Houben, and W.A. Serdijn, "The evolution of pacemakers," *IEEE Eng. Med. Biol. Magazine*, vol. 25, no. 3, pp. 38 - 48, May 2006.

[9] M. Ghovanloo and S. Atluri, "An integrated full-wave CMOS rectifier with built-in back telemetry for RFID and implantable biomedical applications," *IEEE Trans. Circuits Syst. I*, vol. 55, no. 10, pp. 3328-3334, Nov. 2008.

[10] M. Catrysse, B. Hermans, and R. Puers, "An inductive power system with integrated bidirectional data-transmission," *Sens. Actuators A*, vol. 115, pp. 221-229, 2004.

[11] M. Ghovanloo and K. Najafi, "A wireless implantable multichannel microstimulating system-on-a-chip with modular architecture," *IEEE Trans. Neural Sys. Rehab. Eng*., vol. 15, no. 3, pp. 449-457, Sept. 2007.

[12] C. Sauer, M. Stanacevic, G. Cauwenberghs, and N. Thakor, "Power harvesting and telemetry in CMOS for implanted devices," *IEEE Trans. Circuits Syst. I*, vol. 52, no. 12, pp. 2605-2613, Dec. 2005.

[13] T. Fujii and Y. Ibata, "Effects of heating on electrical activities of guinea pig olfactory cortical slices," *Eur. J. Physiol*., vol. 392, pp. 257-260, 1982.

[14] W. X. Zhong, X. Liu, and S. Y. R. Hui, "A novel single-layer winding array and receiver coil structure for contactless battery charging systems with free-positioning and localized charging features," *IEEE Trans. Ind. Elect*., vol. 58, no. 9, pp. 4136-4144, Sept. 2011.

[15] K. Finkenzeller, *RFID-Handbook*, 2nd ed. Hoboken, NJ: Wiley, 2003.

[16] Near Field Communication (NFC) Forum, [online]. Available: http://www.nfc-forum.org
[17] U. Jow and M. Ghovanloo, "Design and optimization of printed spiral coils for efficient transcutaneous inductive power transmission," *IEEE Trans. Biomed. Circuits Syst*., vol. 1, no. 3, pp. 193-202, Sept. 2007.
[18] M. Ghovanloo and K. Najafi, "Fully integrated wideband high-current rectifiers for inductively powered devices," *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 1976-1984, Nov. 2004.
[19] M. Sawan, Y. Hu, and J. Coulombe, "Wireless smart implants dedicated to multichannel monitoring and microstimulation," *IEEE Circuits and Systems Magazine*, vol. 5, no. 1, pp. 21-39, 2005.
[20] J. V. Ham and R. Puers, "A power and data front-end IC for biomedical monitoring systems," *Sens. Actuators A*, vol. 147, no. 2, pp. 641-648, Oct. 2008.
[21] P. Cong, N. Chaimanonart, W. H. Ko, and D. J. Young, "A wireless and batteryless 10-bit implantable blood pressure sensing microsystem with adaptive RF powering for real-time laboratory mice monitoring," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3631-3644, Dec. 2009.
[22] P. Li and R. Bashirullah, "A wireless power interface for rechargeable battery operated medical implants," *IEEE Trans. Circuits Syst. II*, vol. 54, no. 10, pp.912-916, Oct. 2007.
[23] T. Le, J. Han, A. Jouanne, K. Marayam, and T. Fiez, "Piezoelectric micro-power generation interface circuits," *IEEE J. Solid-State Circuits*, vol. 41, no. 6, pp. 1411-1420, June 2006.
[24] T. Umeda, H. Yoshida, S. Sekine, Y. Fujita, T. Suzuki, and S. Otaka, "A 950-MHz rectifier circuit for sensor network tags with 10-m distance," *IEEE J. Solid-State Circuits*, vol. 41, no. 1, pp. 35-41, Jan. 2006.
[25] H. Nakamoto, D. Yamazaki, T. Yamamoto, H. Kurata, S. Yamada, K. Mukaida, T. Ninomiya, T. Ohkawa, S. Masui, and K. Gotoh, "A passive UHF RF identification CMOS tag IC using ferroelectric RAM in 0.35-µm technology," *IEEE J. Solid-State Circuits*, vol. 42, no. 1, pp. 101-110, Jan. 2007.
[26] K. Kotani, A. Sasaki, and T. Ito, "High-efficiency differential-drive CMOS rectifier for UHF RFIDs," *IEEE J. Solid-State Circuits*, vol. 44, no. 11, pp. 3011-3018, Nov. 2009.
[27] J. Yoo, L. Yan, S. Lee, Y. Kim, and H. Yoo, "A 5.2mW self-configured wearable body sensor network controller and a 12?W 54.9% efficiency wirelessly powered sensor for continuous health monitoring system," *IEEE J. Solid-State Circuits*, vol. 45, no. 1, pp. 178-188, Jan. 2010.
[28] F. Mounaim and M. Sawan, "Integrated high-voltage inductive power and data-recovery front end dedicated to implantable devices," *IEEE Trans. Biomed. Circuits Syst.* vol. 5, no. 3, pp. 283-291, June 2011.
[29] Y. H. Lam, W. H. Ki, and C. Y. Tsui, "Integrated low-loss CMOS active rectifier for wirelessly powered devices," *IEEE Trans. Circuits Syst. II*, vol. 53, no. 12, pp.1378-1382, Dec. 2006.
[30] G. Bawa and M. Ghovanloo, "Active high power conversion efficiency rectifier with built-in dual-mode back telemetry in standard CMOS technology," *IEEE Trans. Biomed. Circuits Syst.*, vol. 2, no. 3, pp. 184-192, Sept. 2008.

[31] S. Guo and H. Lee, "An efficiency-enhanced CMOS rectifier with unbalanced-biased comparators for transcutaneous-powered high-current implants," *IEEE J. Solid-State Circuits*, vol. 44, no. 6, pp. 1796-1804, June 2009.
[32] S. Hashemi, M. Sawan, and Y. Savaria, "A novel low-drop CMOS active rectifier for RF-powered devices: Experimental results," *Microelectronics Journal*, vol. 40, iss. 11, pp. 1547-1554, Jan. 2009.
[33] T. Lehmann and Y. Moghe, "On-chip active power rectifiers for biomedical applications," in *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS)*, May 2005, pp. 732-735.
[34] N. J. Guilar, R. Amirtharajah, and P. J. Hurst, "A full-wave rectifier with integrated peak selection for multiple electrode piezoelectric energy harvests," *IEEE J. Solid-State Circuits*, vol. 44, no. 1, pp. 240-246, Jan. 2009.
[35] C. Peters, D. Spreemann, M. Ortmanns, and Y. Manoli, "A CMOS integrated voltage and power efficient AD/DC converter for energy harvesting applications," *J. Micromech. Microeng*., vol. 18, iss. 10, pp. 104005, Oct. 2008.
[36] Y. Hwang and H. Lin, "A new CMOS analog front end for RFID tags," *IEEE Trans. Ind. Electron.*, vol. 56, no. 7, pp. 2299-2307, July 2009.
[37] T. Y. Man, P. K. T. Mok, and M. J. Chan, "A 0.9-V input discontinuous-conduction-mode boost converter with CMOS-control rectifier," *IEEE J. Solid-State Circuits*, vol. 43, no. 9, pp. 2036-2046, Sept. 2008.
[38] E. Sackinger, A. Tennen, D. Shulman, B. Wani, M. Rambaud, D. Lim, F. Larsen, and G. S. Moschytz, "A 5-V AC-powered CMOS filter- selectivity booster for POTS/ADSL splitter size reduction," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2877-2884, Dec. 2006.
[39] Q. Li, R. Zhang, Z. Huang, and Y. Inoue, "A low voltage CMOS rectifier for wirelessly powered devices," in Proc. *IEEE Int. Symp. Circuits and Systems (ISCAS)*, May 2010, pp. 873-876.
[40] G. Bawa, A. Huang, and M. Ghovanloo, "An efficient 13.56 MHz active back-telemetry rectifier in standard CMOS technology," in Proc. *IEEE Int. Symp. Circuits and Systems (ISCAS)*, May 2010, pp. 1201-1204.
[41] K. F. E. Lee, "High-voltage rectifier and voltage doubler in conventional 0.18µm CMOS process," in *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS)*, May 2010, pp. 605-608.
[42] Y. Lu, W.-H. Ki, and J. Yi, "A 13.56MHz CMOS rectifier with switched-offset for reversion current control," *IEEE Symp. VLSI Circuits*, June 2011, pp. 246-247.
[43] E. Dallago, D. Miatton, G. Venchi, V. Bottarel, G. Frattini, G. Ricotti, and M. Schipani, "Active autonomous AC-DC converter for piezoelectric energy scavenging systems," in *Proc. IEEE Custom Integrated Circuits Conference (CICC)*, Sept. 2008, pp. 555-558.
[44] S. Cheng, Y. Jin, and D. Arnold, "An active voltage doubling ac/dc converter for low-voltage energy harvesting applications," *IEEE Trans. Power Elec*., vol. 26, no. 8, pp. 2258-2265, Aug. 2011.
[45] E.S. Krames, P.H. Peckham, and A.R. Rezai, Eds., *Neuromodulation*. Oxford: Elsevier Ltd., 2009.
[46] F. Shahrokhi, K. Abdelhalim, D. Serletis, P. Carlen, and R. Genov, "The 128-channel fully differential digital integrated neural recording and stimulation

interface," *IEEE Trans. on Biomed. Circuits and Systems*, vol. 4, no. 3, pp. 149-161, June 2010.
[47] K. Chen, Z. Yang, L. Hoang, J. Weiland, M. Humayun, and W. Liu, "An integrated 256-channel epiretinal prosthesis," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1946-1956, Sept. 2010.
[48] A.M. Kuncel and W.M. Grill, "Selection of stimulus parameters for deep brain stimulation," *Clin. Neurophysiol*., vol. 115, iss. 11, pp. 2431-2441, Nov. 2004.
[49] D.R. Merrill, M. Bikson, and J.G.R. Jefferys, "Electrical stimulation of excitable tissue: design of efficacious and safe protocols," *J. Neuroscience Methods*, vol. 141, pp. 171-198, Feb. 2005.
[50] S.K. Moore, "Psychiatry's shocking new tools," *IEEE Spectrum*, vol. 43, issue 3, pp. 24-31, Mar. 2006.
[51] H.C.F. Martens, E. Toader, M.M.J. Decre, D.J. Anderson, R. Vetter, D.R. Kipke, K.B. Baker, M.D. Johnson, J.L. Vitek, "Spatial steering of deep brain stimulation volumes using a novel lead design," *Clin. Neurophysiol*., vol. 122, iss. 3, pp. 558-566, Mar. 2011.
[52] J. Vidal and M. Ghovanloo, "Toward a switched-capacitor based stimulator for efficient deep-brain stimulation," in *Proc. IEEE Eng. in Med. and Biol. Conf. (EMBC)*, pp. 2927-2930, Sept. 2010.
[53] J. Simpson and M. Ghovanloo, "An experimental study of voltage, current, and charge controlled stimulation front-end circuitry," in *Proc. IEEE Intl. Symp. on Cir. and Sys. (ISCAS)*, pp. 325-328, May 2007.
[54] S. Kelly and J. Wyatt, "A power-efficient neural tissue stimulator with energy recovery," *IEEE Trans. Biomed. Circuits Syst*., vol. 5, no. 1, pp. 20-29, Feb. 2011.
[55] M. Kiani, U. Jow, and M. Ghovanloo, "Design and optimization of a 3-coil inductive link for efficient wireless power transmission," *IEEE Trans. Biomed. Circuits Syst*., vol. 5, no. 6, pp. 579-591, Dec. 2011.
[56] R. Xue, K. Cheng, and M. Je, "High-efficiency wireless power transfer for biomedical implants by optimal resonant load transformation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 4, pp. 867-874, Apr. 2013.
[57] K. F. E. Lee, "A timing controlled AC-DC converter for biomedical implants," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2010, pp. 128-129.
[58] S. Arfin and R. Sarpeshkar, "An energy-efficient, adiabatic electrode stimulator with inductive energy recycling and feedback current regulation," *IEEE Trans. Biomed. Circuits Syst*., vol. 6, no. 1, pp. 1-14, Feb. 2012.
[59] E. Noorsal, K. Sooksood, H. Xu, R. Hornig, J. Becker, and M. Ortmanns, "A neural stimulator frontend with high-voltage compliance and programmable pulse shape for epiretinal implants," *IEEE J. Solid-State Circuits*, vol. 47, no. 1, pp. 244-256, Jan. 2012.
[60] H. Xu, E. Noorsal, K. Sooksood, J. Becker, and M. Ortmanns, "A multichannel neurostimulator with transcutaneous closed-loop power control and self-adaptive supply," in *IEEE Eur. Solid-Stats Circuits Conf. (ESSCIRC)*, Sept. 2012.
[61] A. Wongsarnpigoon, J. P. Woock, and W. M. Grill, "Efficiency analysis of waveform shape for electrical excitation of nerve fibers," *IEEE Trans. Neural Syst. Rehab. Eng*., vol. 18, no. 3, pp. 319-328, June 2010.

[62] A. Wongsarnpigoon and W. M. Grill, "Energy-efficient waveform shapes for neural stimulation revealed with a genetic algorithm," *J. Neural Eng*., vol. 7, no. 4, June 2010.
[63] S. Masui, E. Ishii, T. Iwawaki, Y. Sugawara, and K. Sawada, "A 13.56-MHz CMOS RF identification transponder integrated circuit with a dedicated CPU," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 1999, pp. 162-163.
[64] G. Bawa and M. Ghovanloo, "Analysis, design and implementation of a high efficiency fullwave rectifier in standard CMOS technology," *Analog Integrated Circuits and Signal Processing*, vol. 60, pp. 71-81, Aug. 2009.
[65] S. B. Lee, H. Lee, M. Kiani, U. Jow, and M. Ghovanloo, "An inductively powered scalable 32-ch wireless neural recording system-on-a-chip with power scheduling for neuroscience applications," *IEEE Trans. Biomed. Circuits Syst*., vol. 4, no. 6, pp. 360–371, Dec. 2010.
[66] Diodes Inc. "1N4148WT data sheet," [Online] www.diodes.com/datasheets/ ds30396.pdf
[67] H. K. Cha, W. T. Park, and M. Je, "A CMOS rectifier with a cross-coupled latched comparator for wireless power transfer in biomedical applications," *IEEE Trans. Circuit Syst. II, Exp. Briefs*, vol. 59, no. 7, pp. 409–413, Jul. 2012.
[68] U. Jow and M. Ghovanloo, "Modeling and optimization of printed spiral coils in air, saline, and muscle tissue environments," *IEEE Trans. Biomed. Circuits Syst*., vol. 3, no. 5, pp. 339-347, Oct. 2009.
[69] H. Park, M. Kiani, H.-M. Lee, J. Kim, J. Block, B. Gosselin, and M. Ghovanloo, "A wireless magnetoresistive sensing system for an intraoral tongue-computer interface," *IEEE Trans. Biomed. Circuits Syst*., vol. 6, no. 6, pp. 571-585, Dec. 2012.
[70] M. Kiani, and M. Ghovanloo, "An RFID-based closed loop wireless power transmission system for biomedical applications," *IEEE Trans. Circuits Syst. II*, vol. 57, no. 4, pp. 260-264, Apr. 2010.
[71] G. Lazzi, "Thermal effects of bioimplants," *IEEE Eng. Med. Biol. Mag*., vol. 24, no. 5, pp. 75–81, Sep./Oct. 2005.
[72] J. Thelin, H. Jörntell, E. Psouni, M. Garwicz, J. Schouenborg, N. Danielsen, and C. E. Linsmeier, "Implant size and fixation mode strongly influence tissue reactions in the CNS," *PLoS One*, vol. 6, no. 1, pp. e16267-e16267, Jan. 2011.
[73] X. Liu, A. Demosthenous, A. Vanhoestenberghe, D. Jiang, and N. Donaldson, "Active Books: The Design of an Implantable Stimulator That Minimizes Cable Count Using Integrated Circuits Very Close to Electrodes," *IEEE Trans. Biomed. Circuits Syst*., vol. 6, no. 3, pp. 216-227, Jun. 2012.
[74] I. H. Ibrahim and J. L. Parker, "Multi-electrode cochlear implant system with distributed electronics," European Patent 2335774A1, Jun. 22, 2011.
[75] M. Duncan, I. Bruinsma, Z. Milijasevic, and A. Barriskill, "Distributed functional electrical stimulation system," U.S. Patent 7127287B2, Oct. 24, 2006.
[76] D. Andreu, D. Guiraud, and G. Souquet, "A distributed architecture for activating the peripheral nervous system," *Journal of Neural Engineering*, vol. 6, no. 2, Apr. 2009.

[77] M. T. Gerber and W. D. Weimer, "Neurostimulation system with distributed stimulators," U.S. Patent 20060020297, Jan. 26, 2006.
[78] K. Iniewski, *VLSI Circuits for Biomedical Applications*, 1st ed. Norwood, MA: Artech House, 2008.
[79] J.-J. Sit and R. Sarpeshkar, "A low-power blocking-capacitor-free charge-balanced electrode-stimulator chip with less than 6 na dc error for 1-ma full-scale stimulation," *IEEE Trans. Biomed. Circuits Syst*., vol. 1, no. 3, pp. 172–183, Sep. 2007.
[80] K. Sooksood, T. Stieglitz, and M. Ortmanns, "An active approach for charge balancing in functional electrical stimulation," *IEEE Trans. Biomed. Circuits Syst*., vol. 4, no. 3, pp. 162–170, Jun. 2010.
[81] Texas Instruments, "MSP430F2132 data sheet," [Online] www.ti.com/product/ msp430f2132
[82] X. F. Wei and W. M. Grill, "Impedance characteristics of deep brain stimulation electrodes in vitro and in vivo," *J. Neural Eng*., vol. 6, no. 4, Aug. 2009.
[83] V. Valente, A. Demosthenous, R. Bayford, "A tripolar current-steering stimulator ASIC for field shaping in deep brain stimulation," *IEEE Trans. Biomed. Circuits Syst.*, vol. 6, no. 3, pp. 197–207, Jun. 2012.
[84] DBS 3387, 3389 lead kit for deep brain stimulation, Medtronic, Minneapolis, MN, 2010.
[85] S. Kim, P. Tathireddy, R. A. Normann, and F. Solzbacher, "Thermal impact of an active 3-D microelectrode array implanted in the brain," *IEEE Trans. Neural Sys. Rehab. Eng*., vol. 15, no. 4, pp. 493-501, Dec. 2007.
[86] Federal Communications Commission (FCC), "Questions and answers about biological effects and potential hazards of radiofrequency electromagnetic fields," *OET Bulletin 56*, August 1999.
[87] M. Ghovanloo, "Switched-capacitor based implantable low-power wireless microstimulating systems," in *Proc. IEEE Intl. Symp. on Cir. and Sys. (ISCAS)*, pp. 2197-2200, May 2006.
[88] F. Zhang, A. Aravanis, A. Adamantidis, L. de Lecea, and K. Deisseroth, "Circuit-breakers: optical technologies for probing neural signals and systems," *Nature Reviews Neuroscience*, vol. 8, no. 8, pp. 577–581, Aug. 2007.
[89] V. Gilja, V. Gilja, C. A. Chestek, C. A. Chestek, I. Diester, I. Diester, J. M. Henderson, J. M. Henderson, K. Deisseroth, K. Deisseroth, K. V. Shenoy, and K. V. Shenoy, "Challenges and opportunities for next-generation intracortically based neural prostheses," IEEE *Trans. Biomed. Eng*, vol. 58, no. 7, pp. 1891–1899, Jul. 2011.
[90] C. T. Wentz, J. G. Bernstein, P. Monahan, A. Guerra, A. Rodriguez, and E. S. Boyden, "A wirelessly powered and controlled device for optical neural control of freely-behaving animals," *J. Neural Eng*., vol. 8, no. 4, Jun. 2011.
[91] S. Paul, A.M. Schlaffer, and J.A. Nossek, "Optimal charging of capacitors," *IEEE Trans. Circuits Syst. I*, vol. 47, no. 7, pp. 1009-1016, Jul. 2000.
[92] B. D. Valle, C. T. Wentz, and R. Sarpeshkar, "An area and power- efficient analog Li-ion battery charger circuit," *IEEE Trans. Biomed. Circuits Syst*., vol. 5, no. 2, pp. 131–137, Apr. 2011.

[93] M. Chen and G. A. Rincon-Mora, “Accurate, compact, and power- efficient Li-ion battery charger circuit,” *IEEE Trans. Circuits Syst. II,* vol. 53, no. 11, pp. 1180–1184, Nov. 2006.
[94] J. J. Chen, F. C. Yang, C. C. Lai, Y. S. Hwang, and R. G. Lee, “A high-efficiency multimode Li-Ion battery charger with variable current source and controlling previous-stage supply voltage,” *IEEE Trans. Ind. Electron.,* vol. 56, no. 7, pp. 2469–2478, Jul. 2009.
[95] K. Kwon, B. Sirowatka, A. J. Weber, and W. Li, “Opto-μECoG array: A hybrid neural interface with transparent μECoG electrode array and integrated LEDs for optogenetics,” *IEEE Trans. Biomed. Circuits Syst.,* vol. 7, no. 5, pp. 593-600, Oct. 2013.
[96] K. Kwon, A. Khomenko, M. Haq, and W. Li, " Integrated slanted microneedle-LED array for optogenetics," in *Proc. IEEE Eng. in Med. and Biol. Conf. (EMBC),* pp. 249-252, Jul. 2013.
[97] C. C. McIntyre, A. G. Richardson, and W. M. Grill, “Modeling the excitability of mammalian nerve fibers: Influence of afterpotentials on the recovery cycle,” *J. Neurophysiol*. vol. 87, no. 2, Feb. 2002.
[98] E. N. Warman, W. M. Grill, and D. Durand, “Modeling the effects of electric fields on nerve fibers: Determination of excitation thresholds,” *IEEE Trans. Biomed. Eng*. vol. 39, no. 12, pp. 1244-1254, Dec. 1992.
[99] C. R. Butson and C. C. McIntyre, "Tissue and electrode capacitance reduce neural activation volumes during deep brain stimulation," *Clin. Neurophysiol*., vol. 116, iss. 10, pp. 2490-2500, Oct. 2005.
[100] C. C. McIntyre, S. Mori, D. L. Sherman, N. V. Thakor, and J. L. Vitek, “Electric field and stimulating influence generated by deep brain stimulation of the subthalamic nucleus,” *Clin. Neurophysiol.* vol. 115, iss. 3, pp. 589-595, Mar. 2004.
[101] H.-M. Lee and M. Ghovanloo, “An integrated power-efficient active rectifier with offset-controlled high speed comparators for inductively-powered applications,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 8, pp. 1749-1760, Aug. 2011.
[102] H.-M. Lee and M. Ghovanloo, "An adaptive reconfigurable active voltage doubler/rectifier for extended-range inductive power transmission," *IEEE Trans. Circuits Syst. II*, vol. 59, no. 8, pp.481-485, Aug. 2012.
[103] H.-M. Lee and M. Ghovanloo, “A high frequency active voltage doubler in standard CMOS using offset-controlled comparators for inductive power transmission,” *IEEE Trans. Biomed. Circuits Syst.*, vol. 7, no. 3, pp. 213-224, Jun. 2013.
[104] H.-M. Lee, H. Park, and M. Ghovanloo, "A power-efficient wireless system with adaptive supply control for deep brain stimulation," *IEEE J. Solid-State Circuits*, vol. 48, no. 9, pp. 2203-2216, Sep. 2013.
[105] H.-M. Lee and M. Ghovanloo, "A power-efficient wireless capacitor charging system through an inductive link," *IEEE Trans. Circuits Syst. II*, vol. 60, no. 10, pp. 707-711, Oct. 2013.
[106] H.-M. Lee and M. Ghovanloo, “Fully integrated power-efficient AC-to-DC converter design in inductively-powered biomedical applications,” in *Proc. IEEE Custom Integrated Circuits Conference (CICC)*, Sep. 2011.

[107] H.-M. Lee and M. Ghovanloo, "An adaptive reconfigurable active voltage doubler/rectifier for extended-range inductive power transmission," in *IEEE Int. Solid-State Circuits Conf. (ISSCC)*, pp. 286-287, Feb. 2012.

[108] H.-M. Lee, K.-Y. Kwon, W. Li, and M. Ghovanloo, "A power-efficient switched-capacitor stimulating system for electrical/optical deep-brain stimulation," accepted for presentation in *IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2014.

[109] S. B. Lee, H.-M. Lee, M. Kiani, U.-M. Jow, and M. Ghovanloo, "An inductively powered scalable 32-ch wireless neural recording system-on-a-chip with power scheduling for neuroscience applications," in *IEEE Int. Solid-State Circuits Conf. (ISSCC)*, pp. 120-121, Feb. 2010.

[110] H. Park, B. Gosselin, M. Kiani, H.-M. Lee, J. Kim, X. Huo, and M. Ghovanloo, "A wireless magnetoresistive sensing system for an intra-oral tongue-computer interface," in *IEEE Int. Solid-State Circuits Conf. (ISSCC)*, pp. 124-125, Feb. 2012.

[111] K.-Y. Kwon, H.-M. Lee, M. Ghovanloo, A. Weber, and W. Li, "A wireless slanted optrode array with integrated micro LEDs for optogenetics," accepted for presentation in *IEEE Int. Conf. Micro Electro Mechanical Systems (MEMS)*, Jan. 2014.